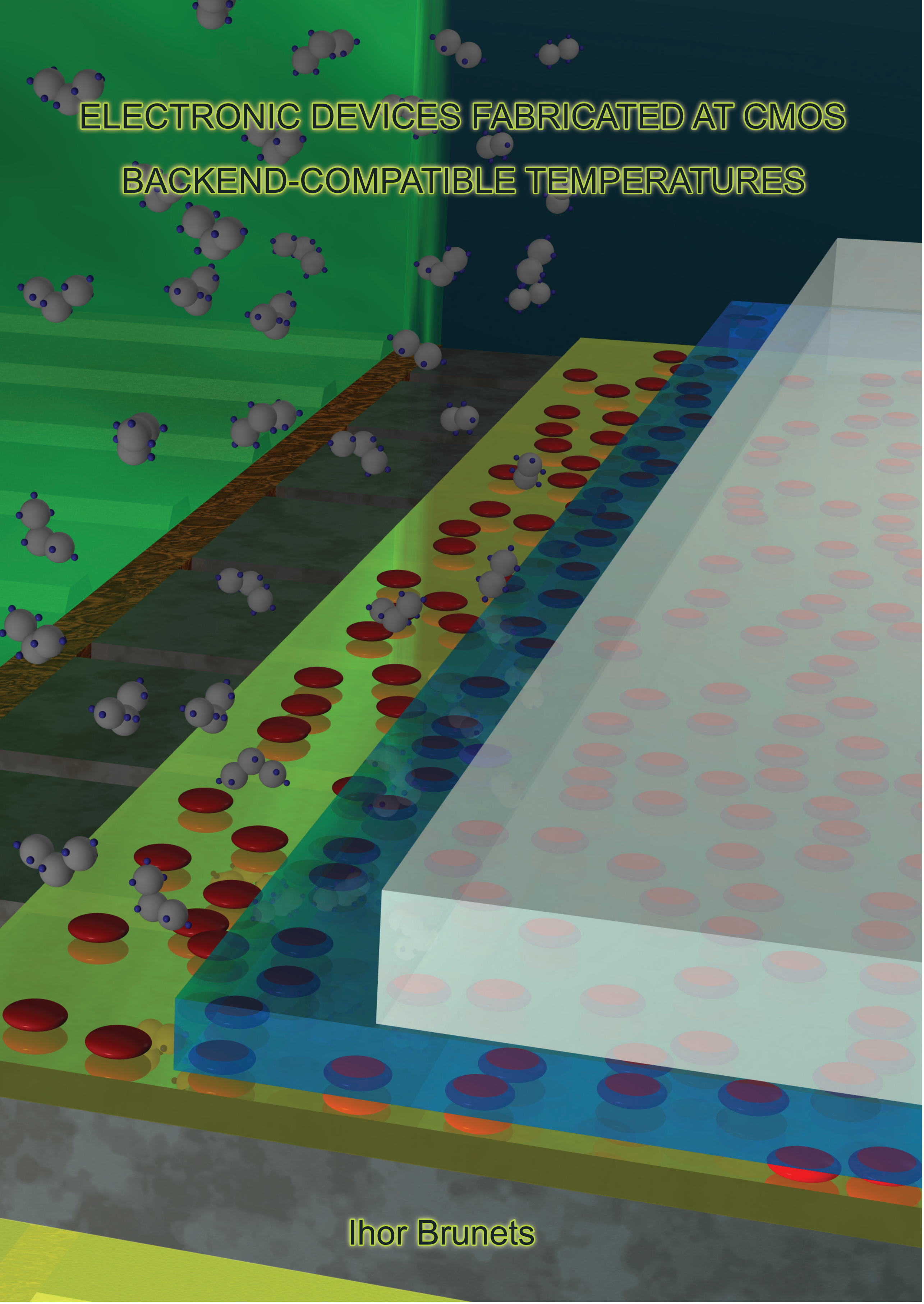

ELECTRONIC DEVICES FABRICATED AT CMOS BACKEND-COMPATIBLE TEMPERATURES

Ihor Brunets

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Cover: illustration of the main process steps described in the dissertation: green-laser crystallization of preformed *a*-Si film and deposition of functional multilayer stack (SiO_2, Si-nanodots, Al_2O_3, Al-metallization).

Cover design: Oleg Vorobyov

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ELECTRONIC DEVICES FABRICATED AT CMOS BACKEND-COMPATIBLE TEMPERATURES

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ter verkrijging van de graad van doctor

aan de Universiteit Twente

op gezag van de Rector Magnificus

prof. dr. H. Brinksma

volgens besluit van het College voor Promoties

in het openbaar te verdedigen

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dr. J. Holleman (assistant promoter)

To my family.

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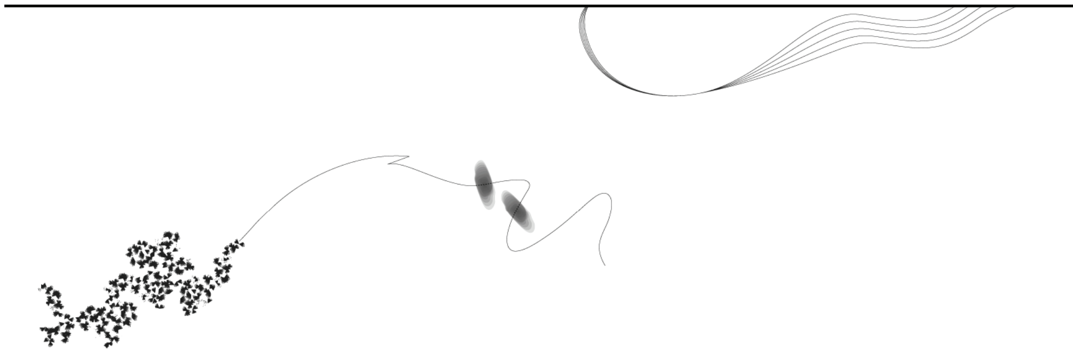
"No Exponential Is Forever:
But "Forever" Can Be Delayed!"

Gordon E. Moore
(International Solid State Circuits Conference, Feb. 10, 2003)

1 General introduction



1.1 3-D integration prolongs Moore's Law

The semiconductor industry experienced a tremendous technology development over the last half century. Until now it was possible to follow Moore's law [1] by scaling down the device dimensions and in the same time remaining a planar platform of integrated circuits (IC). It was achieved mainly by improvement of lithographic processes leading nowadays to nanometre-dimensions in complementary metal-oxide-semiconductor (CMOS) technology.

Although the industry is expected to follow the scaling road for at least another 10-15 years, further downscaling becomes much more challenging due to the several technical and commercial difficulties. The continuous dimensional scaling successively improved the transistor performance in terms of gate switching delay; however the global interconnect resistance-capacitance (RC) delay has gradually become the main circuit performance limiting factor. Additionally, the chip area enlargement necessary to facilitate the increased functionality leads to an enormous increase of the total interconnect length. As a result it will cause significant power dissipation problems deteriorating the performance of the ICs. Therefore, further functionality growth within conventional planar ICs would not be possible without compromising on performance, process complexity, or cost.

The perspective for using the third dimension not only for interconnects but also for introducing of the next active layers (i.e. device layers) was already envisaged by Feynman in his lecture "There's Plenty of Room at the Bottom," held at the annual meeting of the American Physical Society (California Institute of Technology, December 29, 1959) and published in 1960 [2]. So, three-dimensional (3-D) integration of ICs could be an effective solution to circumvent RC delay bottlenecks in today's interconnect-dominated chip performance.

An illustrative example of the semiconductor industry segment, which experiences a strong demand for development of a revolutionary fabrication process, is the memory market. Increase of bit capacity of the memory chips

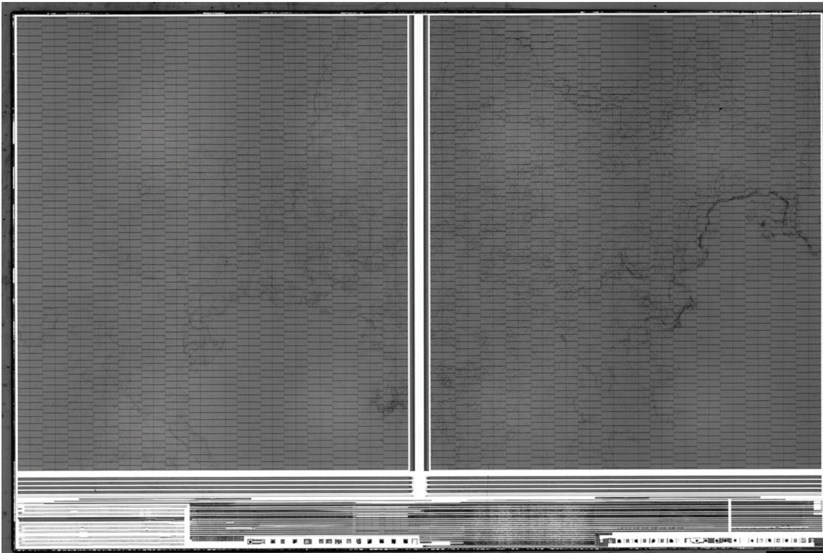


Figure 1.1: Die Photograph of the Toshiba 56 nm 16 Gb NAND Flash (Source: Semiconductor Insights, 2007)

while keeping their compactness is achieved by following Moore's law also in memory cell design, similar to other IC technologies. However, flash memory downsizing is reaching its physical barriers earlier in comparison to downscaling in other integrated devices (e.g. problems with scaling of the blocking and especially tunnelling dielectrics, etc.). In the meantime, the size of the memory array increases in comparison to the size of the periphery due to aggressively increased bit capacity (see Figure 1.1). Therefore, memory chip development already now drives towards lower thermal budgets, and aims at 3-D integration [3-10].

There are a number of approaches available for a 3-D IC integration, so called post-singulation packaging or chip stacking (also known as chip-to-chip), and pre-singulation wafer-level integration (e.g. chip-to-wafer, wafer-to-wafer and full monolithic integration) [3, 7, 8, 10-16]. Each approach uses different alignment methods, bonding techniques etc., offering different vertical interconnect densities, and hence a various degree of improvement of ICs.

1.2 Aims of this work

In this work we will focus on process steps required for the monolithic 3-D integration of ICs. In this approach, vertical integration of several active layers is done by their sequential processing starting from the bottommost device layer (shown in Figure 1.2). To avoid degradation of underlying devices, this approach demands tight thermal budgets during the formation of each next active layer and further device processing. Figure 1.3 gives a general overview of typical process temperatures for state-of-the-art technologies compared with several commonly used processing steps.

Therefore, the following technology key-points were investigated intensively:

- low-temperature deposition of semiconductor and dielectric films;
- grain boundary location controlled crystallization of the silicon films and dopant activation using a green laser.

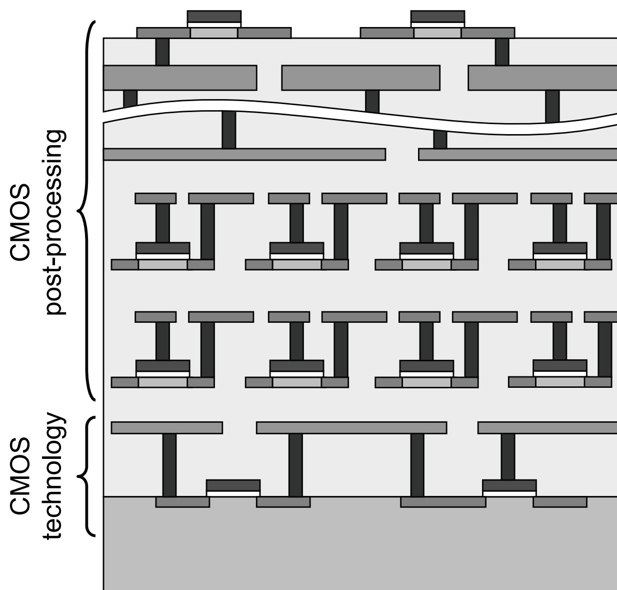


Figure 1.2: Monolithic 3-D integration of IC.

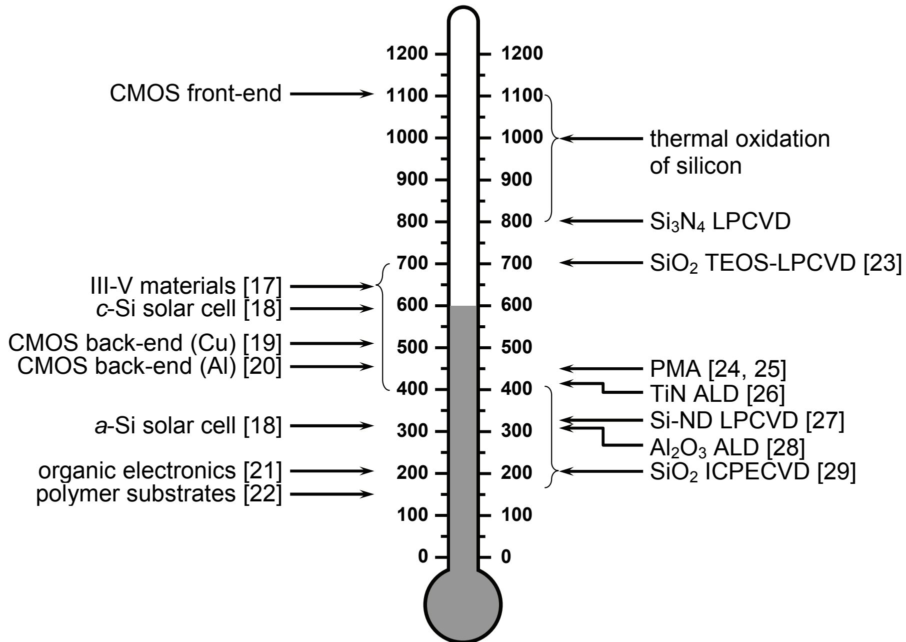


Figure 1.3: Typical process temperatures for state-of-the-art technologies.

The performance advantages provided by the mentioned process steps are demonstrated using electronic devices realized at CMOS backend-compatible temperatures, i.e. temperatures well below 450 °C.

1.3 Outline of the thesis

Chapter 2

Chapter 2 gives a general overview of the equipment used in this work for fabrication and analysis of the realized structures. The design of a cluster system and the development of deposition modes available to form low temperature semiconductor and dielectric layers are described. Then, the laser equipment used for crystallization and dopant activation in silicon films is shown. The description of measurement and analysis techniques employed in this work finalize the chapter.

Chapter 3

An important issue during device processing is the formation of semiconducting and dielectric layers. The techniques used in this work, such as oxidation, various types of chemical vapour deposition, atomic layer deposition, are described in chapter 3. The processing of the multilayer structures for memories and photonic applications is reported.

Chapter 4

This chapter deals with deposition and characterization of silicon nanodots - the key element of the realized memory cells and light emitting devices. The influence of the precursor gases, reactor conditions and substrate material on the silicon nucleation and film growth mechanisms are discussed in detail. Layers with high surface density of nanodots required for good memory performance are reported.

Chapter 5

Chapter 5 presents the devices with embedded silicon nanodots realized at low processing temperatures. Advantages of the discontinuous floating gate for 3-D integrated memories are discussed. The performance of the memory cells with a layer of silicon nanodots as a floating gate is investigated. Optical characterisation of the functional multilayer stack with silicon nanodots embedded in an alumina matrix completes this chapter.

Chapter 6

In this chapter a novel approach to make high-performance CMOS at low temperatures is presented. It starts with a brief overview of TFT technology development followed by a short description of silicon laser crystallization methods. The demand on grain boundary control in crystallized films is explained. It is proposed to use a pre-formed amorphous silicon film, which allows to predict the locations of the random grain boundaries after crystallization. Due to the simplicity of this method (i.e. it uses only available processing steps) it could be easily implemented in 3-D

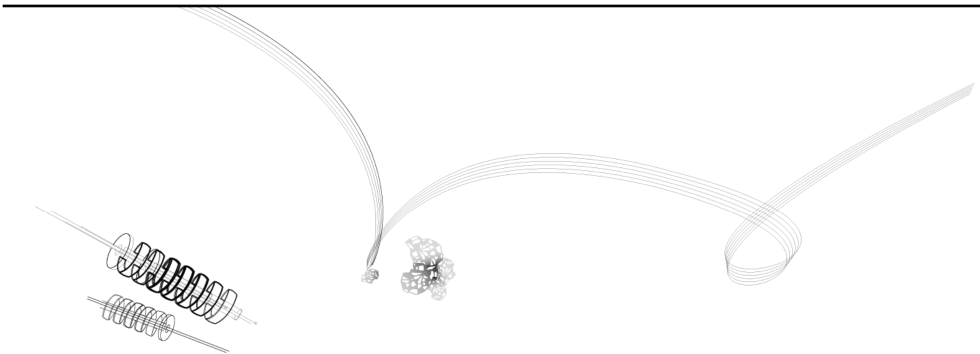
integration. Numerous results of green-laser annealing employed for crystallization and dopant activation are presented. Sheet resistance measurements of anisotropic silicon films are interpreted and the dopant activation level is estimated. The recombination processes in crystallized films are modelled and the experimental data analysed. Fully functional electronic devices (i.e. TFTs, CMOS inverters and ring oscillators) manufactured at back-end compatible substrate temperatures on crystallized silicon films are demonstrated. They are extensively characterized and the results are discussed.

“Per varios usus artem experientia fecit”

“Through different exercises practice
has brought skill”

Marcus Manilius

2 Experimental



2.1 Introduction

This chapter contains a general overview of various specific equipment used in this work. First, the design and capability of the cluster deposition system are described. Then, the laser system used for silicon film crystallization and dopant annealing is presented. The second part of the chapter gives a short description of the measurement and analysis techniques used (i.e., spectroscopic ellipsometer, equipment for the electrical measurements, photo- and electroluminescence set-up).

2.2 Design of the cluster reactor

The deposition of the gate dielectrics (SiO_2, Al_2O_3), silicon nanodot layers and passivation/metallization layers (TiN) was done in a cluster system consisting of three single-wafer reactors connected via a shared loadlock, shown in Figure 2.1. This design allows us to combine different techniques for the sequential deposition of various layers without vacuum break, preventing the undesirable reaction of deposited films with air. Reactor 1 is used for inductively coupled remote plasma enhanced chemical vapour deposition (ICPECVD) and is aimed at deposition of nanocrystalline-Si and *a*-Si layers, as well as dielectric films. This reactor can also operate in an atomic layer deposition (ALD) or ICP-ALD mode. Reactors 2 and 3 operate either in a chemical vapour deposition (CVD) or ALD mode. Reactor 2 is used for the deposition of silicon, metal layers, and metal nitrides. Reactor 3 is mainly used as an ALD reactor for Al_2O_3.

The deposited layer thicknesses were determined with a Woollam M2000U spectroscopic ellipsometer described in section 2.4. The SE could be used in an "*ex-situ*" and "*in-situ*" (only in reactor 1) mode as well as in a "*close-coupled*" mode. *Close-coupled* means that deposition takes place in reactor 2 or 3 and that thickness is measured by transferring the wafer to reactor 1 without vacuum break.

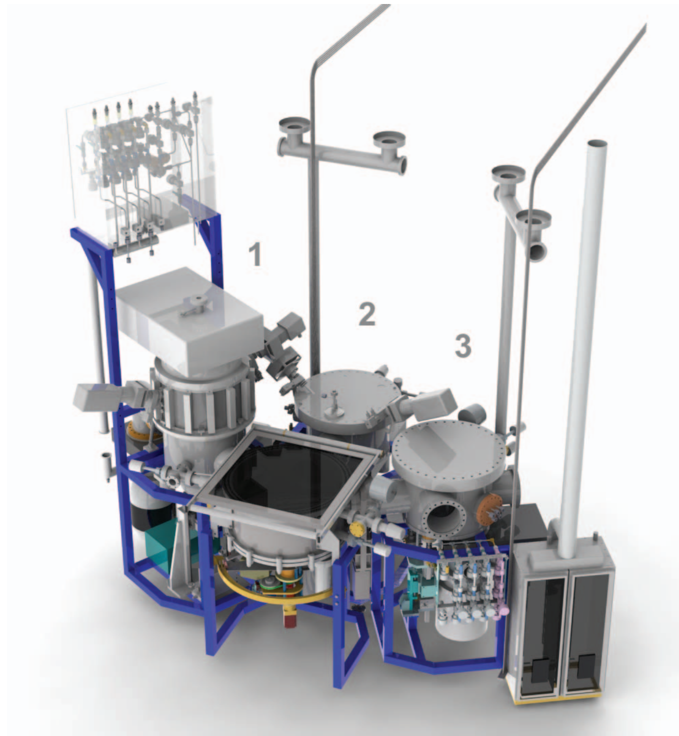


Figure 2.1: Cluster system.
Reactor 1: ICPECVD for low-temperature deposition.
Reactor 2: deposition of metals and silicon in ALD and CVD modes.
Reactor 3: deposition of Al_2O_3.

The cluster system further includes two experimental LPCVD batch reactors, as shown in Figure 2.2. The loadlock, three single-wafer reactors and the two LPCVD batch reactors are PC-controlled, using a Labview application. This application provides the control of all pneumatic gas valves, the throttle valves, the valves for sample transport, the turbo pump controllers, the temperature controllers. The read-out data of the pressure, temperature and gas-flow sensors is displayed on the interface. Pneumatic gas valves are used in a common gas system to provide the five reactors with a choice of 20 semiconductor technology gases. Additionally, these pneumatic valves are used to pulse the reactive gases for the ALD process.

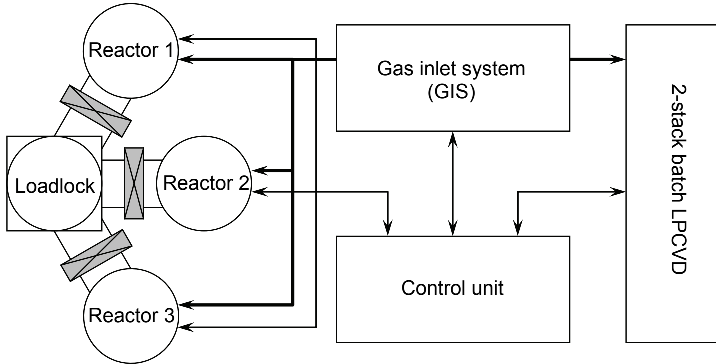


Figure 2.2: Schematic drawing of the cluster system.

2.3 Laser crystallization equipment

The silicon films were crystallized using the laser optical system LAVA available at INNOVAVENT GmbH, utilizing a green (515 or 532 nm) laser beam up to 54 mm length. A schematic block diagram of the optical system is shown in Figure 2.3.

The laser beam has a uniform top-hat profile along the *x*-direction and a

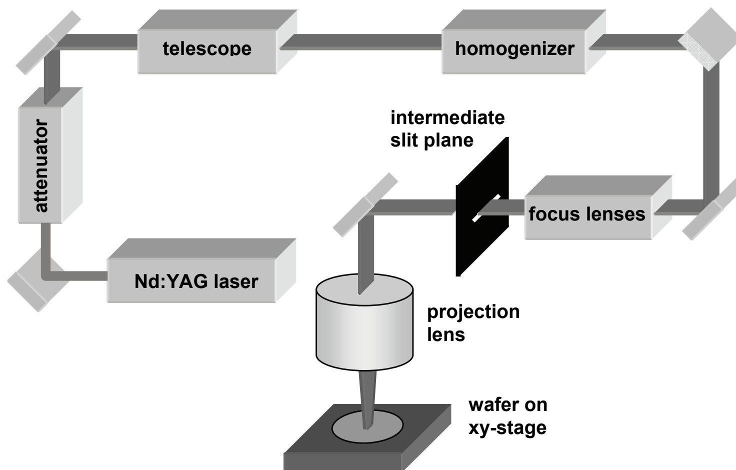


Figure 2.3: Block diagram of the laser optical system.

Gaussian profile along the (scanning) *y*-direction (see Figure 2.4). The beam intensity profile was measured at the wafer plane using a CCD camera and a 40× microscope. The average energy density in the beam was adjusted by an optical attenuator. The energy density was defined as the total pulse energy divided by the Full-Width Half-Maximum (FWHM) area of the beam [30-32].

For the film crystallization, we used the second harmonic of a diode-pumped Yb:YAG thin disk laser (model JenLas® ASAMA) irradiating at a repetition rate of 50 kHz. The pulse duration was 206 ns. The applied beam length was 8 mm and the width was 5.8 µm, both FWHM values. The scan velocity was varied between 1 and 6 mm/s providing a beam overlap of 90 - 98 %. To define and shape the line edges, an adjustable mechanical slit embedded in the intermediate slit plate was used. It was imaged on the wafer surface with a 10× demagnification. Silicon film crystallization was investigated at laser energy densities ranging from 0.6 J/cm^2 to 1.2 J/cm^2.

The dopant activation was done by a laser optical system similar to that used for the crystallization. The applied laser energy density was 0.4 J/cm^2; the beam length was 5.16 mm and the width was 28.4 µm. The pulse duration was 300 ns with a repetition rate of 10.2 kHz, and the scan velocity

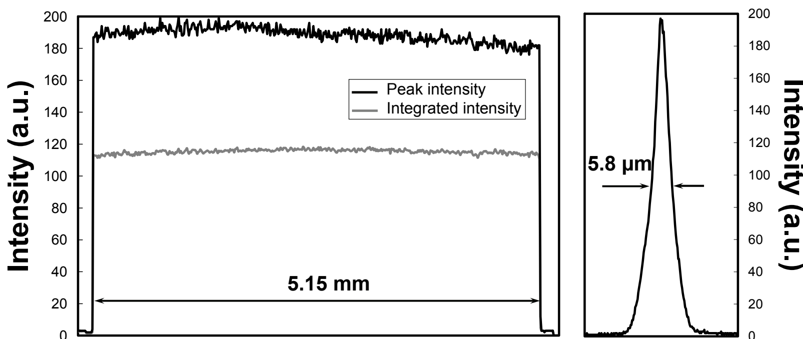


Figure 2.4: Laser beam intensity profiles: (a) along the x axis (perpendicular to the scanning direction) and (b) along the y axis (parallel to the scanning direction).

Treatment	Silicon crystallization	Dopant activation
Wavelength (nm)	515	515
Laser energy density (J/cm^2)	0.6 – 1.2	0.4
Beam length (mm)	8	5.16
Beam width (µm)	5.8	28.4
Pulse duration (ns)	206	300
Repetition rate (kHz)	50	10.2
Scan velocity (mm/s)	1 - 6	14.5
Beam overlap (%)	98	95

Table 2.1: Laser system settings.

was 14.5 mm/s, providing a beam overlap of 95 %. Under these conditions the dopant becomes active without silicon re-melting.

The summarized settings applied during the silicon film crystallization and dopant activation are shown in Table 2.1.

During the laser treatment the wafer was located on a high accuracy motorized *xy*-stage. The projection lens was mounted on a high precision *z*-stage providing accurate focus adjustment. The depth of focus was ± 10 µm. The adjustment was done by making single pulse imprints on a test wafer followed by optical microscope inspection. The wafer stage, laser shutter and optical attenuator were computer controlled, so that the treatment steps with different energy densities and pulse overlaps were done automatically, at different locations on the wafer.

2.4 Spectroscopic ellipsometry

Ellipsometry is a very sensitive non-destructive surface and thin film optical measurement technique that uses polarized light and measures the polarisation state of the light beam reflected from the sample. Ellipsometry can be used to determine thin film thicknesses and thin film optical constants.

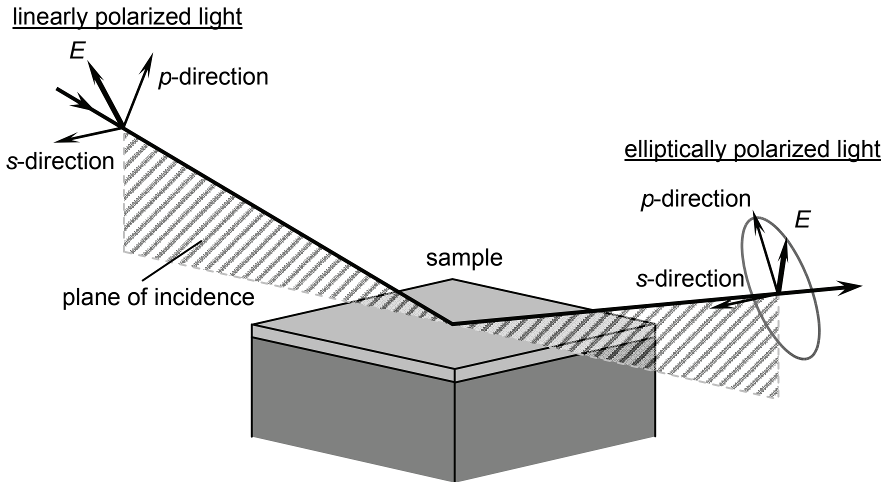


Figure 2.5: Interaction of polarized light with a sample during ellipsometric measurements.

During the ellipsometric measurements an input beam with known linear polarization state is launched onto the sample (as shown in Figure 2.5). The polarization state is described by specifying its components along two orthogonal axes, the so-called *p*- and *s*-directions, in the plane perpendicular to the direction of beam propagation. The *p*-direction is defined as lying in the plane of incidence (which is defined as the plane containing the incident and reflected beams and the vector normal to the sample surface). The s-direction (from Senkrecht, German for perpendicular) lies perpendicular to the *p*-direction. The *p*-direction, *s*-direction, and direction of propagation define a right-handed Cartesian coordinate system.

After reflection from the sample surface it is converted to an elliptically polarized beam. By measuring of the polarization state of the reflected beam values for ellipsometric parameters *psi* (Ψ) and *delta* (Δ) are extracted.

The change in polarization state (ρ) is commonly expressed with Ψ and Δ and defined in (2.1). These values are related to the ratio of Fresnel reflection coefficients $\tilde{R}_p$ and $\tilde{R}_s$ for *p*- and *s*-polarized light, respectively [33].

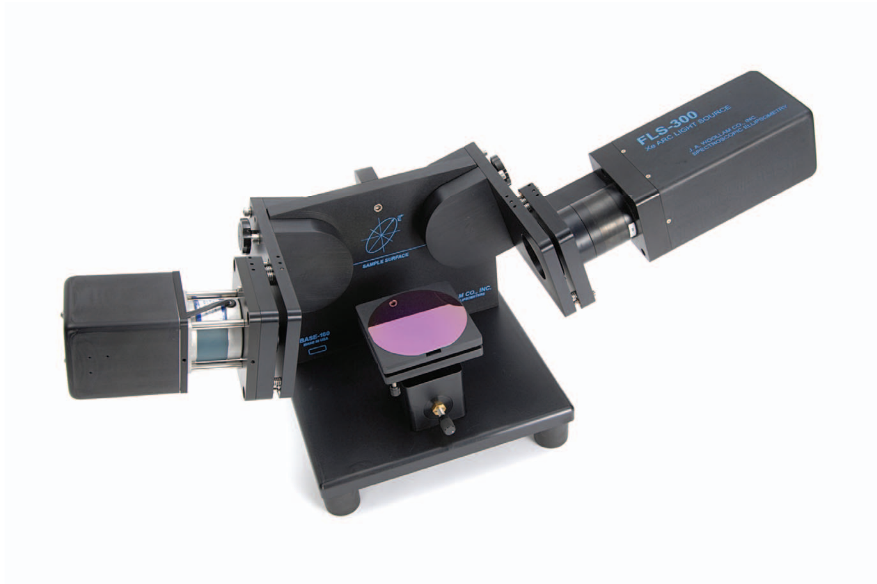


Figure 2.6: Spectroscopic ellipsometer Woollam M2000U in "ex-situ" measurement mode.

$$\rho = \tan(\Psi)e^{i\Delta} = \frac{\tilde{R}_p}{\tilde{R}_s} \tag{2.1}$$

In other words, tan(Ψ) is the magnitude of the reflectivity ratio, and Δ is the phase.

In Spectroscopic Ellipsometry (SE), *psi* and *delta* values are measured as a function of wavelength. This yields much more information about the

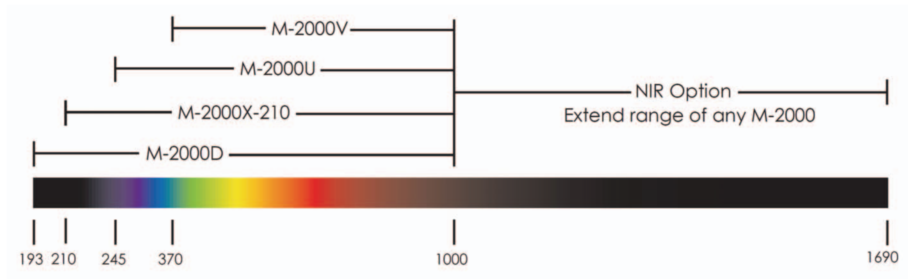


Figure 2.7: Spectral range of various spectroscopic ellipsometer systems.

sample. Therefore, it is possible to analyse the data in specific spectral regions where the required model parameters are more sensitive.

In this work the thickness of the deposited layers was determined by a Woollam M2000U spectroscopic ellipsometer with NIR (near-infrared) option (shown in Figure 2.6). The high-speed CCD detector collects over 700 wavelengths simultaneously, covering the spectral range of 245–1700 nm (Figure 2.7). The M-2000U could be used in "*ex-situ*" mode as shown in Figure 2.6. Additionally, the ellipsometer could be mounted on the process chamber to perform "*in-situ*" thin film monitoring and process control during LPCVD, PECVD, MOCVD, ALD, sputtering, E-beam evaporation, plasma etch, etc.

Thin film parameters such as thickness, optical constants, roughness, composition, etc., were extracted from the measured SE data using CompleteEASE software supplied by J. A. Woollam Co., Inc., which makes use of optical models and tabulated parameters.

2.5 Photo- and electroluminescence measurement setup

Photo- and electroluminescence measurements were performed on samples with silicon nanodots embedded in Al_2O_3, deposited at low-temperature using ALD (see Chapter 3). The optical measurements were done in the group of Prof. Dr. A. Polman at the FOM-Institute for Atomic and Molecular Physics. The 488 nm line of an argon-ion laser was used for excitation of the nanodots. The excitation power was typically 1 W/cm^2. The emitted light was collected with a f = 25 mm lens (NA = 0.45). Then the sample's emission spectrum was measured with a spectrograph Acton SP2300 equipped with a Si CCD-detector PIXIS:400B, both from Princeton Instruments. Quantum efficiency of the CCD detector is shown in Figure 2.8. A low-pass filter, placed in front of the spectrograph entrance slit was used to block the excitation wavelength [34].

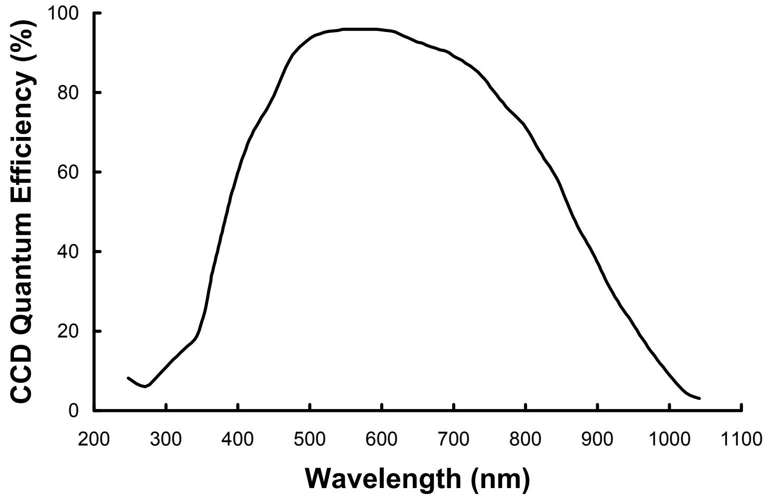


Figure 2.8: Quantum efficiency of back-illuminated Si CCD-detector PIXIS:400B with permanent deep thermoelectric cooling.

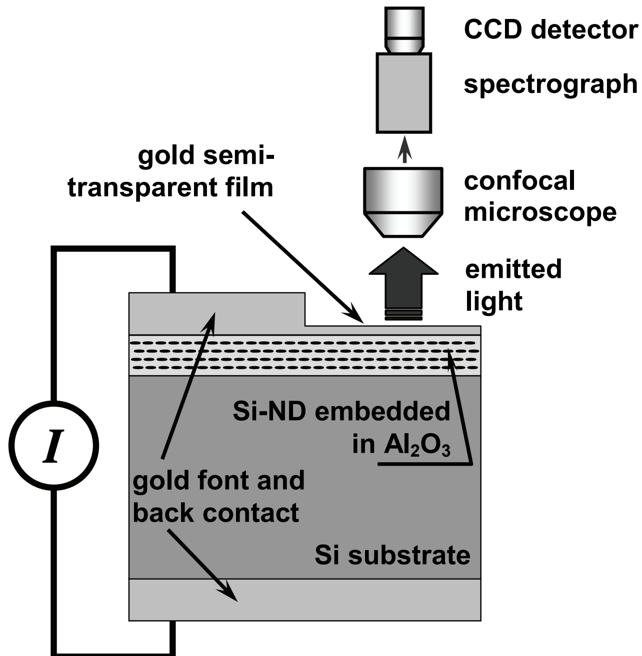


Figure 2.9: Schematic overview of the electroluminescence measurement set-up.

The electroluminescence was measured on the metal-insulator-silicon capacitor structures. A schematic cross-sectional set-up overview is shown in Figure 2.9. Samples with up to 4 layers of silicon nanodots embedded in alumina were investigated. To enable measuring the emitted light, a 20-nm thick semi-transparent layer of gold was additionally sputtered on the top surface (i.e. directly on the Al_2O_3/Si-NC layer stack). Then the electrically contacted sample was mounted under an inverted scanning confocal microscope. When biasing a sample the Si nanodots were excited by impact excitation [35] and the electroluminescence signal was measured.

2.6 Electrical measurements

Electrical measurements, including *C-V* and *I-V* characterisations, sheet resistance, static and dynamic characteristics of CMOS inverters were performed on a Karl Suss MicroTec PM300 Manual Probe Station equipped

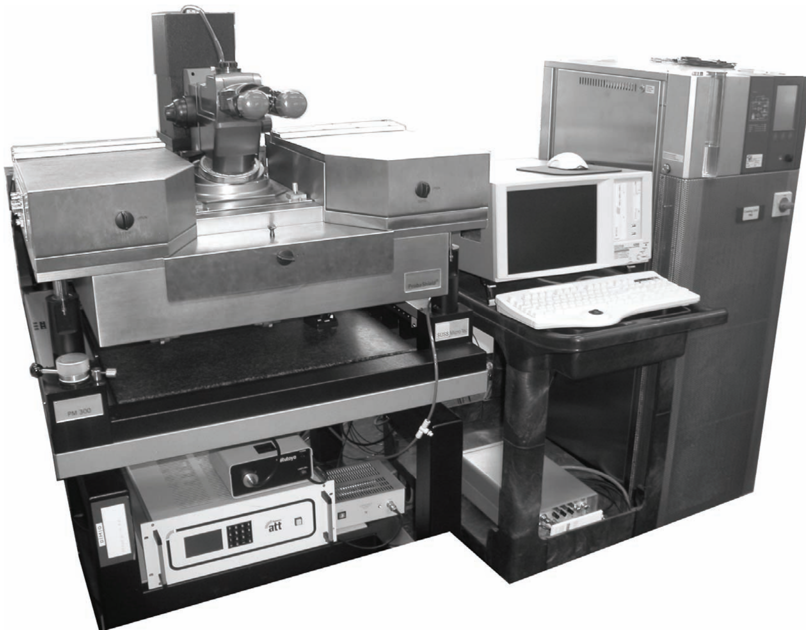


Figure 2.10: Karl Suss MicroTec PM300 Manual Probe Station equipped with a Keithley 4200 SCS Semiconductor Characterization System.

with a Keithley 4200 SCS Semiconductor Characterization System including precision remote pre-amplifiers for ultrahigh resolution semiconductor measurements (shown in Figure 2.10). Keithley Interactive Test Environment (KITE) software interface was used to collect and analyse the measured data.

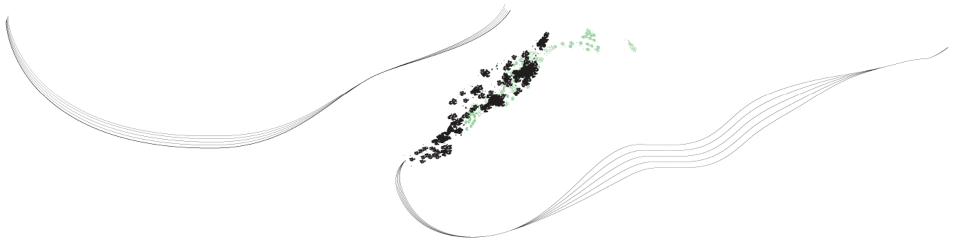
Dynamic characteristics of CMOS ring oscillators were measured using a Tektronix TDS 7404 Digital Phosphor Oscilloscope and HP 4145B Semiconductor Parameter Analyzer.

“Esse est percipi”

“To be is to be perceived”

George Berkeley

3 Formation of functional multilayer stacks



3.1 Introduction

In this chapter a review of the deposition processes used in this work is given. The realised functional multilayer structures for application in floating memories and in light emitting devices are reported. Because a key element of these multilayer stacks, i.e. the layer of silicon nanodots (Si-ND), was investigated intensively, the discussion of Si-ND deposition and characterization is separately treated in Chapter 4.

3.2 Memory cell multilayer structure

Discrete silicon nanodots layer as a replacement for continuous floating gate in conventional non-volatile memories has been intensively studied already since 1996 [36]. Due to their high applicability in 3-D memory chip integration, nanodots deposition techniques gain a lot of attention in today's research [37, 38].

Realized in this work memory cell structures consist of a multilayer of Al/TiN/Al_2O_3/Si-ND/SiO_2/Si. In this stack SiO_2 is the tunnelling dielectric and Al_2O_3 the blocking dielectric. Due to the large difference in dielectric constant *k*, being 3.9 and 9 respectively for SiO_2 and Al_2O_3 the initial field across the SiO_2 is much larger thus creating a Fowler-Nordheim tunnelling through the SiO_2 where the Al_2O_3 is still isolating. This Fowler-Nordheim breakdown however does not only depend on *k* but also on the electron barrier height between Si and dielectric. Since this value is almost equal for SiO_2 and Al_2O_3, *k* values dominate the tunnelling behaviour [39].

Because both thermal SiO_2 and ALD-Al_2O_3, as gate dielectrics are widely used and well-studied materials in integrated silicon devices [40-42], we choose them to be able to concentrate our research on other points, e.g. formation of silicon nanodots layer, etc.

3.2.1 Formation of tunnelling oxide

For memory cells two types of silicon oxide were utilized for tunnelling. 1) A conventional thermal oxide was used as a tunnelling dielectric in non-

volatile memories (described in Chapter 5) and 2) low temperature SiO_2 deposited by means of ICPECVD used as a gate dielectric in TFTs on laser crystallized polysilicon stripes (described in Chapter 6). Before the formation of the oxide layer, a standard cleaning procedure was applied and the native oxide was etched in a solution of 0.3% HF and 0.3% HCl to avoid metal contaminations and to provide a hydrogen-terminated surface.

Thermal oxide

To avoid formation of a low quality non-stoichiometric native oxide, a 2.6-nm thick thermal silicon dioxide layer was grown in a horizontal furnace by means of dry oxidation of the hydrogen-terminated <100> silicon wafer. The sample was loaded at 700°C in N_2 and heated up to 800 °C in N_2, then oxidized at 800 °C in N_2/O_2 (in a ratio of 19:1) and cooled down to 700 °C in N_2 (shown in Figure 3.1). The oxide thickness was determined by the time that the wafer was exposed to the N_2/O_2 ambient. Immediately after oxidation the wafer was transferred to the cluster reactor for further

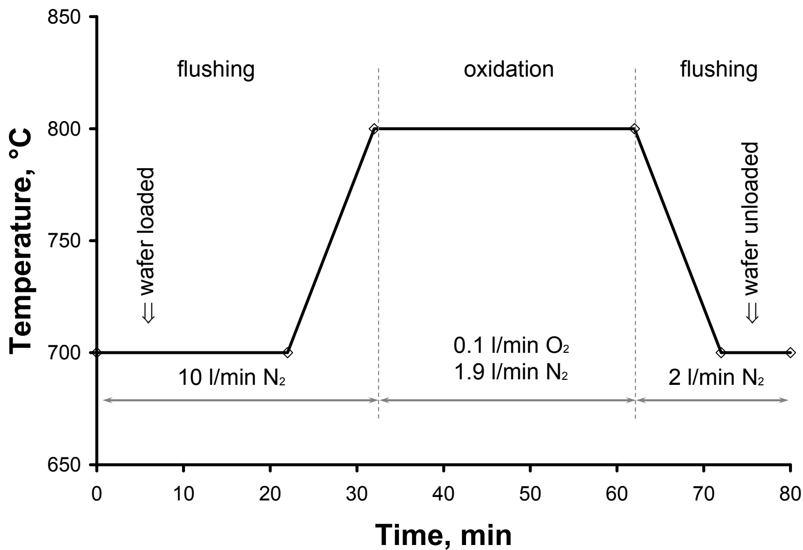


Figure 3.1: Temperature profile used during dry oxidation.

deposition of the functional layers.

For the initial runs of memory stack we used thermal oxide as tunnelling oxide because the SiO_2/Si system is very well known [41, 42] and it gave us the opportunity to investigate the other layers in the memory stack more independently. However, due to the high growth temperature, thermal oxide is not compatible with back-end process, where the temperatures can not exceed 450 °C. So, in a later stage of the research we switched to low temperature ICPECVD silicon oxide.

Low temperature ICPECVD silicon oxide

To maintain a low thermal budget during device fabrication, silicon dioxide gate dielectric layers were deposited in reactor 1 of the cluster system (see section 2.2) using remote inductively coupled plasma-enhanced chemical vapour deposition (ICPECVD) in an Ar-N_2O-SiH_4 plasma at 150 °C and pressure 1 Pa. The gas phase contained 0.08% of SiH_4 and 18% of N_2O - see [43] and [44] for more details. The thickness of the deposited oxides was determined "*in-situ*" by spectroscopic ellipsometer (see section 2.4).

3.2.2 Formation of Silicon Nanodots Layer

After a standard cleaning and short dipping in a solution of 0.3% HF and 0.3% HCl, wafers with thermally grown SiO_2 were loaded into reactor 2 of the cluster system (see section 2.2). In case of the Si-ND deposition on low-temperature layers formed in the cluster system, the wafers were transferred to reactor 2 without any intermedium steps ensuring no vacuum break. Further, the deposition of the functional layer stack (TiN/Al_2O_3/Si-nanodots) was done at temperatures ranging from 300 to 425 °C, without vacuum break. The layer with silicon nanodots was formed by LPCVD at 300-325 °C, using disilane (Si_2H_6) or trisilane (Si_3H_8, known as Silcore®) as the source gases. The deposition pressure ranged between 0.1 and 10 mbar. The deposition parameters, nucleation processes and silicon nanodots layer characterization are discussed in more detail in Chapter 4.

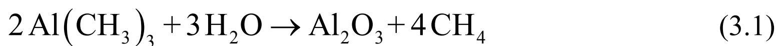
3.2.3 Atomic Layer Deposition of Alumina (Al_2O_3)

Directly after the formation of Si-ND, the wafer was transferred to reactor 3 and covered with an 11-nm thick Al_2O_3 layer (blocking oxide) grown by ALD in 126 cycles at a temperature of 300 °C.

Here it is assumed that the reader knows the basic principles of atomic layer deposition. A good documentation of these deposition techniques may be found in [45-49] and particularly results for ALD of Al_2O_3 in used cluster system in [50].

In general the ALD process of metal oxides is based on sequential exposure of the sample's surface to the oxidizing and reduction precursor gases. In this way, the molecules of the reduction precursor first saturate the available bonding sites on the surface by chemisorption. Then the second precursor is used as an oxidizing agent. So, the ligands of the first precursor molecules are removed from the surface and new bonding states are created. If the gas-phase reaction between both precursors is avoided (e.g., by applying a purge step in-between) the sequential repetition of the described steps leads to the layer-by-layer growth of metal oxide. This provides a precise control over the thickness of the deposited layers, while the deposition rate remains constant (except the starting phase, when the surface has to be completely covered).

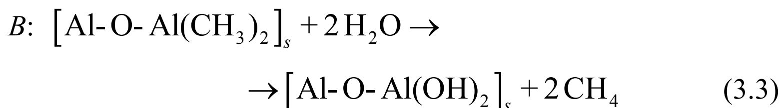
The ALD of Al_2O_3 was based on the overall reaction (3.1) between $Al(CH_3)_3$ (Trimethylaluminum, or TMA) and H_2O:



$$2\,\mathrm{Al}\left(\mathrm{CH_3}\right)_3 + 3\,\mathrm{H_2O} \rightarrow \mathrm{Al_2O_3} + 4\,\mathrm{CH_4} \qquad (3.1)$$

To realize the *ABAB…* sequence of the self-saturating surface reactions (3.2) and (3.3), the wafer was consequently exposed to TMA and H_2O, with a N_2-purge cycle in between [28, 51]:

$$A\!:\ \left[\mathrm{AlOH}\right]_s + \mathrm{Al(CH_3)_3} \rightarrow \left[\mathrm{Al\text{-}O\text{-}Al(CH_3)_2}\right]_s + \mathrm{CH_4} \qquad (3.2)$$



$$B\!:\ \left[\mathrm{Al\text{-}O\text{-}Al(CH_3)_2}\right]_s + 2\,\mathrm{H_2O} \rightarrow$$

$$\rightarrow \left[\mathrm{Al\text{-}O\text{-}Al(OH)_2}\right]_s + 2\,\mathrm{CH_4} \qquad (3.3)$$

were square brackets denote the surface (i.e. adsorbed) species.

The thickness of the deposited layer was measured with a spectroscopic ellipsometer after transferring the wafer to reactor 1 (as described in section 2.4).

3.2.4 Atomic Layer Deposition of Titanium Nitride (TiN)

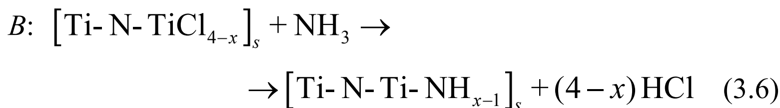
Due to the lower density of ALD-alumina in comparison to the bulk α-Al_2O_3 [50] the weak diffusion of the oxidation species (e.g. water or oxygen) towards the encapsulated Si-ND during further processing steps is possible [52]. To prevent this unwanted diffusion into the blocking Al_2O_3 layer, the wafer was transferred to reactor 2, where a 6-nm thick ALD layer of TiN was deposited in 150 ALD-cycles at 425 °C. The following overall reaction between $TiCl_4$ (Titaniumchloride) and NH_3 has been considered to take place:

$$6\,\mathrm{TiCl_4} + 8\,\mathrm{NH_3} \rightarrow 6\,\mathrm{TiN} + 24\,\mathrm{HCl} + \mathrm{N_2} \qquad (3.4)$$

where ammonia serves as a reducing agent and as a nitrogen source [26, 53-55].

To realize the *ABAB…* sequence of the self-saturating surface reactions, the wafer was consequently exposed to $TiCl_4$ (half-reaction A), followed by the N_2-purge, and to NH_3 (half-reaction B), followed by the same purge. According to (3.4), both HCl and N_2 species are expected to be the volatile byproducts of ALD half-reaction too. However, exclusively HCl formation during deposition cycles was documented and no molecular nitrogen was detected [55]. Therefore, the ALD reaction scheme is better expressed by (3.5) and (3.6):

$$A\colon\ \left[\mathrm{Ti\text{-}NH}_x\right]_s + \mathrm{TiCl_4} \rightarrow \left[\mathrm{Ti\text{-}N\text{-}TiCl}_{4-x}\right]_s + x\,\mathrm{HCl} \qquad (3.5)$$



$$B\colon\ \left[\mathrm{Ti\text{-}N\text{-}TiCl}_{4-x}\right]_s + \mathrm{NH_3} \rightarrow$$

$$\rightarrow \left[\mathrm{Ti\text{-}N\text{-}Ti\text{-}NH}_{x-1}\right]_s + (4-x)\,\mathrm{HCl} \qquad (3.6)$$

where square brackets denote the surface species.

Similarly to the ALD of Al_2O_3 the thickness of the deposited layer was measured with the spectroscopic ellipsometer in reactor 1.

3.2.5 Aluminium sputtering and patterning

Finally, the wafer was removed from the cluster system and both the front- and back-side metallization were realized by sputtering a 1-µm thick aluminium layer in the Oxford PL 400 sputtering system. The sputtering process may lead to significant surface heating [56, 57]. Therefore, to decrease the thermal impact on the multilayer structure the DC power supply was set at 700 W.

Circular MOS capacitors were finally realized by patterning the Al and TiN layers. First the aluminium layer is etched in aluminium-etchant at 55 °C. Then the wafer was rinsed with DI water followed by etching of the TiN at room temperature in approximately 1.5 minute. It was done in a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2), and DI water (H_2O) in a ratio of 1:1:5, also called Standard Clean solution (SC-1) or Ammonia and Hydrogen Peroxide Mixture (APM).

The post metallization furnace anneal was done in a H_2O/N_2 ambient (N_2 bubbling through DI water) for 10 minutes at 400 °C to provide interface dangling bonds passivation. A schematic cross-sectional overview of the realized structure is shown in Figure 3.2.

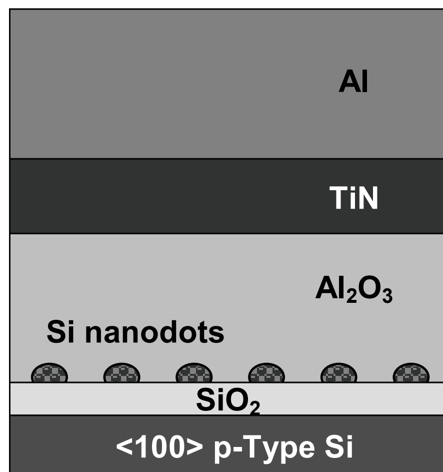


Figure 3.2: A schematic cross-section of the multilayer structure with encapsulated silicon nanodots.

3.3 Light emitting multilayer structure

Light emitting functional multilayer stacks (Al_2O_3/Si-ND/.. /Si-ND/Al_2O_3), consisting of multiple layers of silicon nanodots embedded in an alumina matrix were realized at low temperatures (300-325 °C) by a combination of ALD and CVD techniques.

Immediately after standard cleaning and native oxide etching in a solution of 0.3% HF and 0.3% HCl, the hydrogen-terminated p-type silicon wafers with <100> orientation were loaded into reactor 3 of the cluster

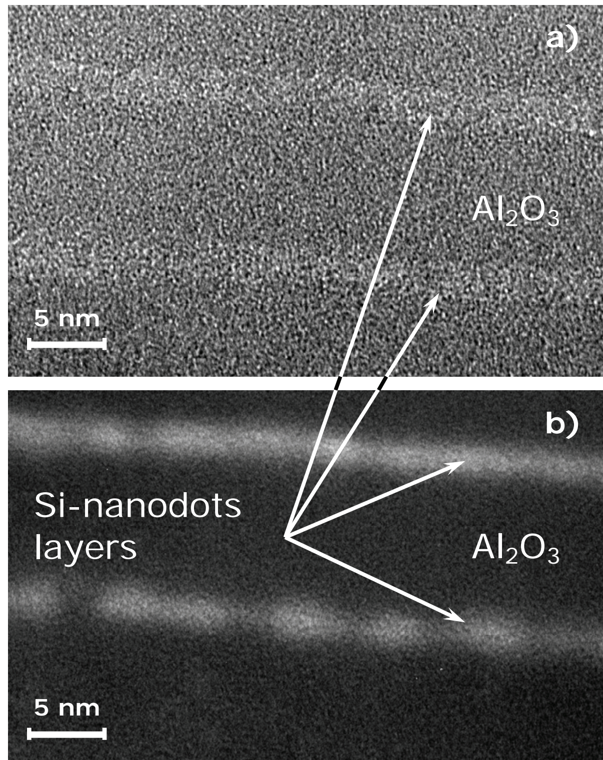


Figure 3.3: High Resolution (a) and Energy Filtered TEM images (b) depicting the cross-section of the multilayer stack with Si-ND embedded in an Al_2O_3 matrix. In the EFTEM image the Si-containing areas appear bright, whereas oxides are dark. It is clearly visible from EFTEM that the Si-ND layers are discontinuous.

system (see section 2.2). There a 10- or 20-nm thick Al_2O_3 layer was grown in respectively 120 or 245 ALD-cycles as described in section 3.2.3. Without vacuum beak, the wafer was transferred to reactor 2, where silicon nanodots were deposited in LPCVD mode from Si_3H_8 at 325 °C and 1 mbar reactor pressure. The deposition time was 30 minutes resulting in 3.5 nm thick Si-nanodots (details are discussed in Chapter 4). This sequence was repeated four times and completed with the last alumina layer.

The realized structures consist of four layers of nanodots embedded in five layers of alumina. Figure 3.3 shows a transmission electron microscope (TEM) image of a cross-section of a structure with 10 nm thick Al_2O_3 layers. The energy filtered TEM analyses confirmed a discontinuous character of the silicon layers.

Finally, the wafer was removed from the cluster system and both the front- and back-side metallization were realized by sputtering gold layers (for the front-side metallization a 20 nm thick semi-transparent gold layer was used to provide enough light transmission and therefore to enable the electroluminescence measurements). A schematic cross-sectional overview of the realized structure is shown in Figure 2.8.

3.4 Conclusions

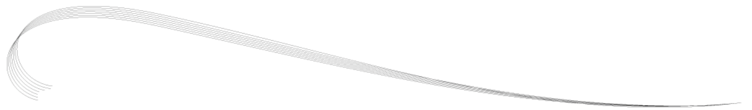
Functional multilayer stacks with embedded Si-ND's were successfully designed and realized by CVD and ALD. The structures used for memory application were fabricated at temperatures below 425 °C except for the thermally grown silicon oxide layer. Optically active multilayer stacks consisting of silicon nanodots embedded in alumina were processed at temperatures below 325 °C. The investigated low temperature multilayer stacks (Al/TiN/Al_2O_3/Si-ND/SiO_2 and Al_2O_3/Si-ND/.. /Si-ND/Al_2O_3) have a potential to be used in 3-D integrated memories [37, 38, 58] and photonic devices [59, 60] (discussed in more detail in Chapter 5).

"Est autem fides credere quod nondum vides;
cuius fidei merces est videre quod credis"

"Faith is to believe what you do not see;
the reward of this faith is to see what you believe"

St. Augustine

4 Deposition of silicon nanodots (Si-ND)



4.1 Introduction

The low-temperature deposition of silicon nanodots being the key element of memory cells and light emitting devices is discussed in this chapter. Formed nanodots layers are characterized using AFM, TEM techniques and spectroscopic ellipsometry. The influence of process parameters on the quality of the nanodot layers is shown.

4.2 Pre-deposition surface treatment

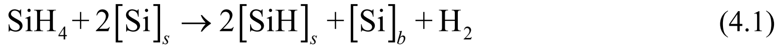
The surface condition plays an important role especially during the starting phase of the deposition process. For the formation of Si nuclei, it is required that the Si precursor itself or intermediate gas phase products react easily with the surface. Reaction with the surface also requires reactive surface sites. To form the required dangling bonds, the dissociation energy of surface Si-O bonds is 4.8 eV while that of surface Si-O-H bonds is significantly lower (1.75 eV) [61]. Due to the large difference in bond energies, hydroxyl groups act as nucleation centres [62] resulting in a much higher nucleation rate of silicon (i.e. higher nanodot density) on a SiO_2 surface terminated by OH groups during the initial phase of LPCVD. In [61, 63] it has been demonstrated that Si nucleation takes place easier on dip etched SiO_2 surfaces, therefore to achieve the surface termination by OH groups and to avoid the metal contaminations, the wafers were briefly (around 1 minute) dipped in a solution of 0.3% HF and 0.3% HCl. Immediately after this dip, the wafers were placed into the loadlock of the cluster system.

4.3 Low Pressure Chemical Vapour Deposition of Si-ND

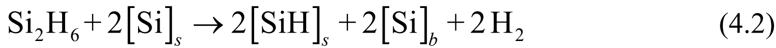
The layer with silicon nanodots was formed by LPCVD in reactor 2 at 300-325 °C, using disilane (Si_2H_6) or trisilane (Si_3H_8, known as Silcore®) as the source gases. The deposition pressure ranged between 0.1 and 10 mbar. The dramatic increase of silicon nucleation and growth rate, when using

Si_3H_8 as a precursor, was reported for deposition temperatures between 410-500 °C [64] and higher. Therefore we expect to obtain a significantly higher Si-ND density using Si_3H_8 instead of Si_2H_6 also at lower temperatures.

Regarding the CVD of silicon, there are three general surface reactions involving Si_2H_6 (4.2), Si_3H_8 (4.3) and SiH_4 (4.1) precursors (schematically shown in Figure 4.1). One should bear in mind that silane can also appear due to gas-phase reactions [65].



$$\mathrm{SiH_4} + 2[\mathrm{Si}]_s \rightarrow 2[\mathrm{SiH}]_s + [\mathrm{Si}]_b + \mathrm{H_2} \quad (4.1)$$



$$\mathrm{Si_2H_6} + 2[\mathrm{Si}]_s \rightarrow 2[\mathrm{SiH}]_s + 2[\mathrm{Si}]_b + 2\,\mathrm{H_2} \quad (4.2)$$

$$\mathrm{Si_3H_8} + 2[\mathrm{Si}]_s \rightarrow 2[\mathrm{SiH}]_s + 3[\mathrm{Si}]_b + 3\,\mathrm{H_2} \quad (4.3)$$

where square brackets with subscription "*s*" denote surface species, whereas subscript "*b*" represents bulk silicon.

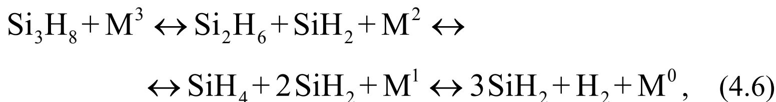
Although the reactivity increases in the order SiH_4 - Si_2H_6 - Si_3H_8, but the reaction probability is rather low for these species at low temperatures due to the very small fraction of the bare surface silicon atoms not covered with hydrogen. In other words, the reactive sticking coefficients of reactions (4.1), (4.2) and (4.3) are very small [66-68], since those direct adsorption mechanisms are defined by the activation energy of surface dehydrogenation (≈ 40 kcal/mol):

$$2[\mathrm{SiH}]_s \rightarrow 2[\mathrm{Si}]_s + \mathrm{H_2}, \quad (4.4)$$

where $[Si]_s$ is the free surface site needed for the surface reactions described above. $[SiH]_s$ is the site occupied by H and therefore not reacting with SiH_4, Si_2H_6 and Si_3H_8. Only at elevated temperatures (higher than 700 °C) the direct adsorption becomes important [69].

At the same time, at sufficient gas pressures the following bimolecular gas-phase reactions sequences can occur [65] during CVD from disilane (4.5) and from silcore (4.6):

$$\mathrm{Si_2H_6} + \mathrm{M}^2 \leftrightarrow \mathrm{SiH_4} + \mathrm{SiH_2} + \mathrm{M}^1 \leftrightarrow 2\,\mathrm{SiH_2} + \mathrm{H_2} + \mathrm{M}^0 \quad (4.5)$$



$$\mathrm{Si_3H_8} + \mathrm{M}^3 \leftrightarrow \mathrm{Si_2H_6} + \mathrm{SiH_2} + \mathrm{M}^2 \leftrightarrow$$
$$\leftrightarrow \mathrm{SiH_4} + 2\,\mathrm{SiH_2} + \mathrm{M}^1 \leftrightarrow 3\,\mathrm{SiH_2} + \mathrm{H_2} + \mathrm{M}^0, \quad (4.6)$$

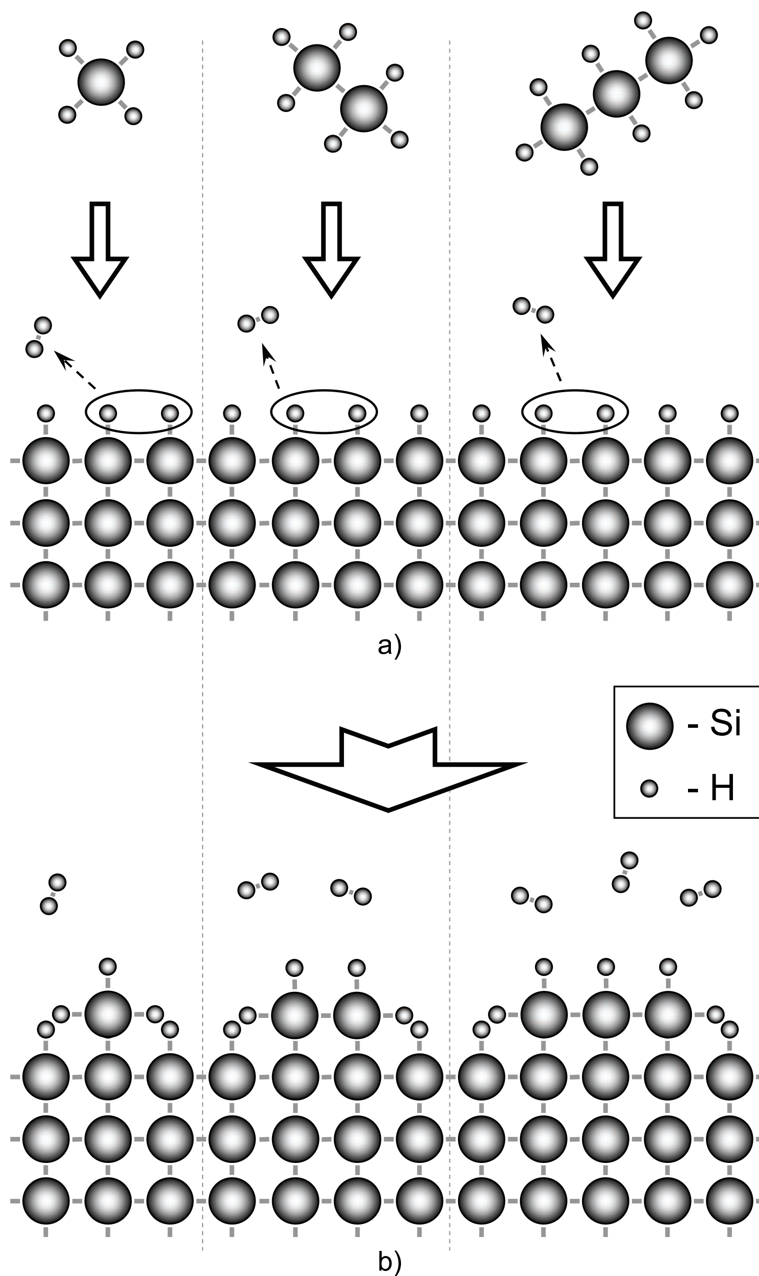


Figure 4.1: General surface reactions during CVD of silicon from silane (SiH_4), disilane (Si_2H_6) and trisilane (Si_3H_8) mainly defined by the activation energy of surface dehydrogenation.

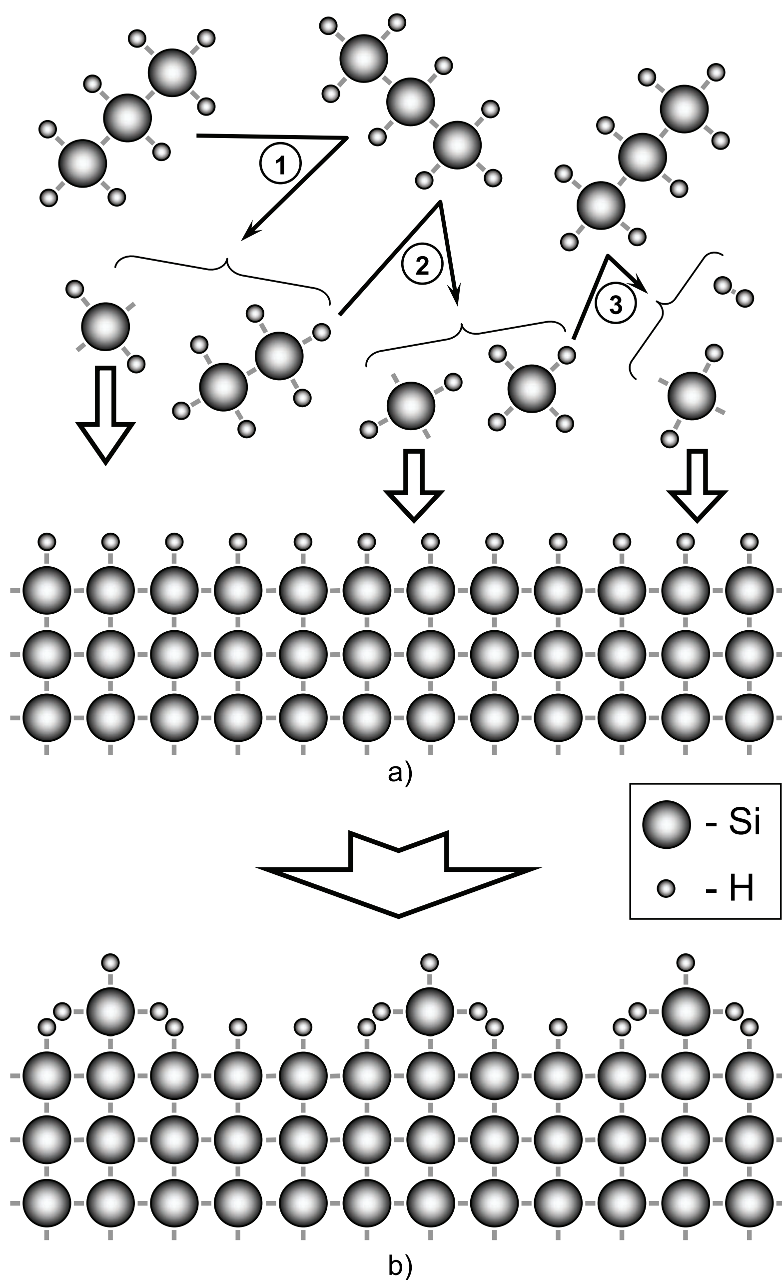
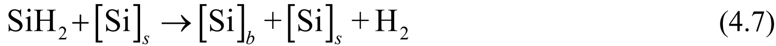


Figure 4.2: Bimolecular gas-phase reaction sequences during CVD of silicon from trisilane (Si_3H_8) and subsequent surface insertion reactions of highly reactive silylene (SiH_2).

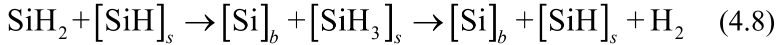
where M^x ($x = 0, 1, 2, 3$) denotes any other gas molecule (as shown in Figure 4.2) and an energy of the molecule M^x is higher than of the molecule M^{x-1}.

As a result, highly reactive species such as SiH_2 (silylene) with a reactive sticking coefficient close to unity are generated [65, 67, 68, 70]. Because of the gas-phase reactions, the rate of silylene formation strongly depends on the total pressure.



$$\mathrm{SiH_2} + [\mathrm{Si}]_s \rightarrow [\mathrm{Si}]_b + [\mathrm{Si}]_s + \mathrm{H_2} \qquad (4.7)$$

This reactive specie can also insert on surface $[SiH]_s$ according to



$$\mathrm{SiH_2} + [\mathrm{SiH}]_s \rightarrow [\mathrm{Si}]_b + [\mathrm{SiH_3}]_s \rightarrow [\mathrm{Si}]_b + [\mathrm{SiH}]_s + \mathrm{H_2} \qquad (4.8)$$

The use of trisilane, according to (4.6), ensures a higher concentration of silylene. Due to the very high reactivity of silylene, it is expected that a higher concentration of silylene will result in a higher nucleation rate providing a higher number of silicon nanodots even on a SiO_2 surface [27].

4.4 Characterization of Si-ND

4.4.1 Spectroscopic Ellipsometry measurements

To investigate the starting phase of silicon nanodots formation during the deposition from trisilane (Si_3H_8) on SiO_2 and Al_2O_3 surfaces, a series of experiments with various deposition times was done. Two types of initial samples were used - with dip-etched thermally grown silicon oxide film and ALD Al_2O_3 film, both 20 nm thick on silicon substrates. Directly after the silicon deposition the layer thickness was measured with the spectroscopic ellipsometer without vacuum break to avoid oxidation of the nanodots.

Besides thickness values also information about the continuity of the nanodot layer was extracted from the SE measurements by using a Maxwell-Garnett Effective Medium Approximation (EMA) of silicon and voids. The samples with Si-ND layers deposited at 1 mbar and 325 °C from trisilane were investigated. The results of deposition on both, silicon- and aluminium oxide surfaces are compared in Figure 4.3.

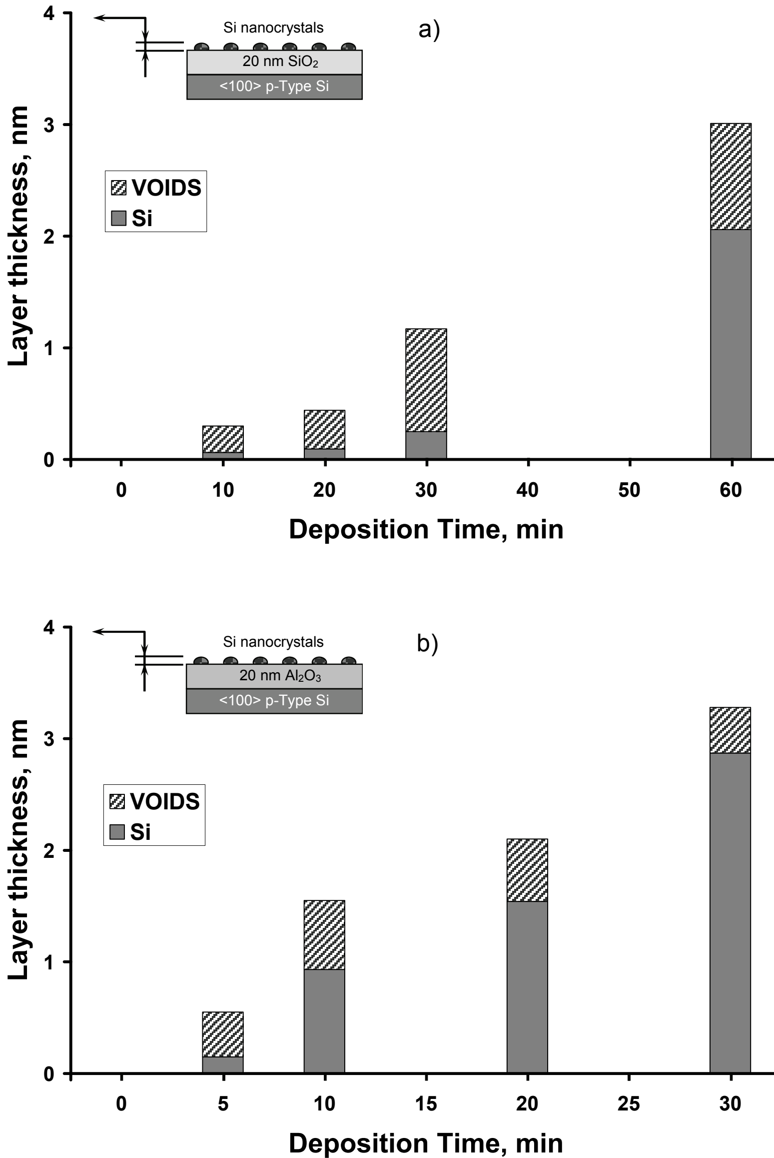


Figure 4.3: Layer thickness and composition extracted from SE measurements using a Maxwell-Garnett Effective Medium Approximation model for Silicon nanodot deposited on SiO_2 (a) and Al_2O_3 (b) surfaces. Deposition conditions: precursor gas flow – trisilane 5 ml/min; pressure - 1 mbar; temperature - 325 °C.

There is a clear difference in the nucleation phase at the beginning of the nanodots layer deposition. Because the LPCVD of nanodots on alumina surface is executed without vacuum break directly after the ALD of Al_2O_3, the surface is fully OH terminated. The hydroxyl groups acting as nucleation centres result in a very high surface density of generated silicon nuclei. Due to the high density of the nanodots layer even at the small nuclei sizes the spectroscopic ellipsometry equipment is sensitive enough to perform an immediate proper measurement (Figure 4.3b).

In contrast to this, when depositing on SiO_2 there is approximately a 20 minute delay before the spectroscopic ellipsometer can measure any significant changes in the nanodots layer (shown in Figure 4.3a). Deceitfully such a delay is called an “incubation time”. However, this term is not completely correct, while the silicon nucleation starts immediately after the exposure of the surface to the precursor gas. Because of an insufficient resolution or sensitivity of the characterisation techniques it is not possible to obtain consistent measurement data from such a layer.

In our case, although the surface of SiO_2 was treated to be -OH terminated (see section 4.2), the number of hydroxyl groups on SiO_2 surface is lower in comparison to the alumina surface [71]. Additionally, the surface may change into Si-O termination during the pre-deposition steps after dipping (e.g., wafer loading, heating up, etc.). The lower surface density of the OH groups leads to the decreased density of generated silicon nucleus. The total volume of nucleated silicon remains negligible in comparison to the space between the dots (i.e., “voids”), therefore no information about Si-ND could be extracted from SE measurements until the ratio Si-ND/voids is below the threshold sensitivity of the equipment. Therefore, in [72] it is proposed to call the described delay as “apparent incubation time”.

To achieve a higher density of Si-nanodots also on SiO_2 surfaces a thin layer of ALD Al_2O_3 (less than 1 nm, i.e., a few ALD cycles) can be formed before deposition of silicon. It acts as a functional surface for the further nucleation of silicon nanodots [73].

4.4.2 AFM characterization

Atomic force microscopy was used to visualize the silicon nanodots after deposition. Samples with nanodots formed on SiO_2 layer were characterized without the covering Al_2O_3 dielectric. We therefore expected the silicon nanodots to be oxidized immediately after exposing them to air (while transporting to the AFM system). Volume expansion during oxidation increases the dimensions of the nanodots, so that the physical size of the nanodots shown in Figure 4.4 is not representative of the encapsulated dots in our floating gate stacks.

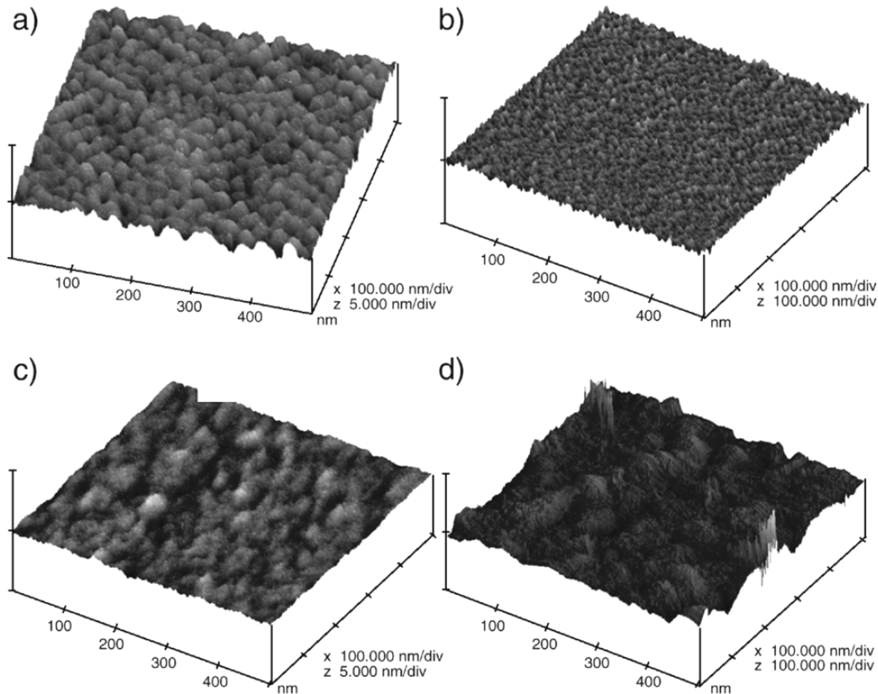


Figure 4.4: The AFM image of oxidized Si-nanodot layers deposited at 325 °C from disilane at 10 mbar (a) and from trisilane at 1 mbar (b), 0.2 mbar (c), 10 mbar (d). To enable the observation of the nanodots, no upper protection layer was deposited. Deposition time 10 minutes.

The AFM surface images of a Si-nanodot layer deposited for 10 minutes at 10 mbar and 325 °C from disilane (Figure 4.4a), and at 1 mbar from trisilane (Figure 4.4b) and show a significantly increased concentration of the nanodots deposited from Silcore (~ 1.9×10^{12} cm^{-2}) in contrast to that deposited from disilane (~ 0.2×10^{12} cm^{-2}) compared in Table 4.1.

Using trisilane, a series of LPCVD experiments at 325 °C and different gas pressures was done. No deposition was observed at 0.2 mbar (see Figure 4.4c) and a very rough and non-uniform nanodot layer (Figure 4.4d) having R_a = 5.39 nm was obtained at 10 mbar of deposition pressure.

For a successful industrial application of the described Si-ND deposition method a high reproducibility together with a high deposition speed is required. However, if the deposition process is very short (i.e. formation of nanodots within a minute), large run-to-run errors will be introduced by the equipment. At the same time, it should be much less than an hour, otherwise the stack growth takes impractically long. Therefore, for Si_2H_6 the 10 mbar, and for Si_3H_8 the 1 mbar could be considered as suitable process pressures during silicon nanodots formation at 325 °C. Due to the obtained higher nanodot density we can conclude that trisilane is a much better choice as a precursor gas for fabrication of Si-ND layers.

	Precursor gas			
	Si_2H_6	Si_3H_8		
Pressure, mbar	10	0.2	1.0	10
Thickness (SE), nm	1.98	0	1.37	16.87
Si-nanodot density, $\times 10^{12}$ cm^{-2}	~ 0.2	0	~ 1.9	~ 0.01
Composition Si/SiO_2	60/40	-	62/38	-
rms, nm	0.25	0.11	2.54	7.10
R_a, nm	0.31	0.08	1.97	5.39

Table 4.1: Characteristics of deposited Si-nanodot layers. Deposition time 10 minutes (no upper protection layer was deposited) at 325 °C.

Ex-situ spectroscopic ellipsometer measurements of the nanodot layers (shown in Figure 4.4) provided us with the information about layer thickness and composition, as listed in Table 4.1.

4.4.3 TEM characterization

Figure 4.5 shows a high resolution top-view TEM image of the multilayer structure with encapsulated Si-nanodots deposited for 10 minutes from disilane at 325 °C and 10 mbar. The observed crystalline features are attributed to the nanodots. They appear to have a crystalline structure and to be oval in shape. The in-plane sizes of the nanodots are in the range of 3 ÷ 8 nm.

4.5 Conclusions

The silicon nanodot layers suitable for application in memories and photonic devices were deposited using LPCVD at low temperatures, satisfying the thermal budget requirements for CMOS post-processing. The expected mechanisms of silicon nucleation and growth are discussed in

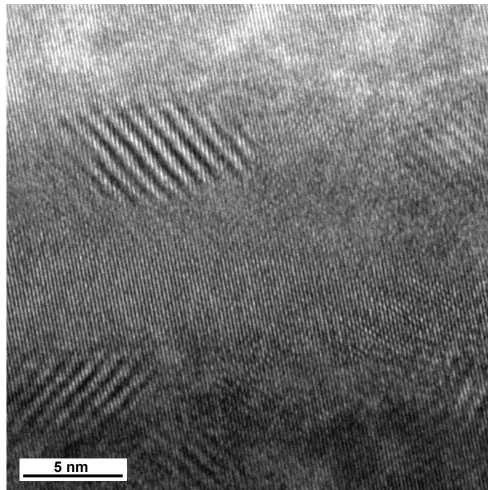


Figure 4.5: High-resolution TEM image displaying nanodots encapsulated into Al_2O_3 dielectric layer

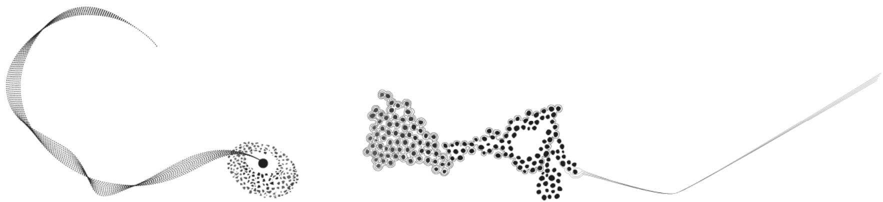
detail. The performed characterization of formed layers (e.g., AFM, TEM, SE) provide information about the obtained high nanodot surface density (up to 1.9×10^{12} cm^{-2}). An increase in the growth rate and in the density of silicon nanodots deposited with Si_3H_8 (Silcore®) as a precursor gas in comparison to Si_2H_6 is demonstrated. Process parameters for obtaining a discrete high-density silicon nanodots layer are discussed. The importance of the substrate material and its surface termination is shown.

“Mater artium necessitas”

“Necessity is the mother of invention”

Πλάτων / Plato

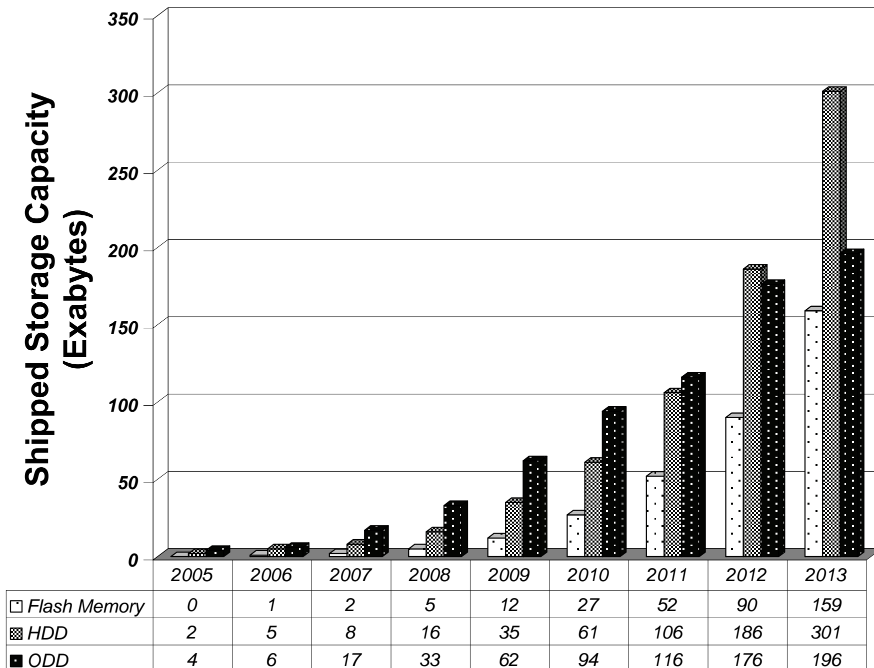
5 Electronic devices with embedded Si-ND



5.1 Introduction

The constantly growing market of portable electronic devices (e.g., mobile phones, digital cameras, data storage devices, notebooks) demands low-cost, high-density, and highly reliable memories (such as SRAM, DRAM, EPROM, EEPROM and flash memories). A particular segment of the flash memories in this marked is rapidly increasing and is expected to approach the capacity volumes of the optical and hard disc drives in the near future (see Figure 5.1).

Comparing the dynamics of memory growth and memory scaling (discussed in section 1.1) one can conclude that there is a strong demand for new memory designs to fulfil today's market requirements. The vertical integration of cell arrays fabricated using processes with low thermal



	2005	2006	2007	2008	2009	2010	2011	2012	2013
Flash Memory	0	1	2	5	12	27	52	90	159
HDD	2	5	8	16	35	61	106	186	301
ODD	4	6	17	33	62	94	116	176	196

Figure 5.1: Total consumer storage usage: optical disc drives (ODD), hard disk drives, and flash memories (Coughlin Associates, January 2008).

budgets, is one of the most promising solutions [4-8].

To overcome the challenges related to low processing temperatures, several new devices are presently investigated as replacements for the traditional floating gate stack; one of which being the nanocrystal memory cell [36-38, 74].

In this chapter an approach to realize silicon nanodot memory cells with a low thermal budget (below 400 °C) is shown. The use of a discontinuous floating gate enables the application of low temperature oxides in the functional multilayer stack, opening the way to 3-D memory structures inside the microchip's backend. The working principle of realized cells and their performance as memory device is discussed here.

Alternatively, photonic devices based on optically active silicon nanodots form another potential application area for Si-ND [59, 60]. Due to their CMOS-compatible processing the Si-ND embedded in an alumina matrix could be used as a light source for the external and internal optical data transfer in integrated circuits. The general optical characteristics of the proposed multilayer system are completing this chapter.

5.2 Non Volatile Memory (NVM)

There is a number of memory types available for non volatile data storage in solid-state circuits such as read-only memory (ROM), programmable read-only memory (PROM), erasable and programmable read-only memory (EPROM), ultraviolet erasable (UVPROM) and electrically erasable (EEPROM). An important subcategory of EEPROM is a flash memory, where the entire memory array or large blocks of the memory array are electrically erased at once. This feature provides faster erase and programming times, smaller cell size and higher cell density (in comparison to EEPROM) leading to lower costs per bit.

The general non volatile memory concept based on modulation of the threshold voltage of the metal-oxide semiconductor field effect transistor (MOSFET) structure, was proposed by I.M. Ross already in 1957 [75]. The next important step was realized in 1967, when D. Kahng and S.M. Sze

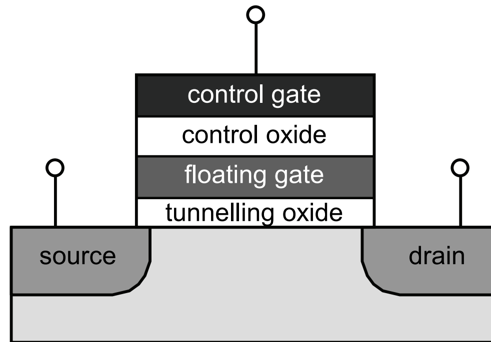


Figure 5.2: Schematic cross-section of the flash memory cell.

reported the first memory device with floating-gate structure [76]. There, an additionally introduced conducting charge trapping layer (floating gate) inside of the gate oxide layer (shown in Figure 5.2) enables a non-volatile information storage mechanism. In the same year, Wegener et al. suggested the use of a Si_3N_4 dielectric with a high charge trap density as charge storage region in MNOS (Metal-Nitride-Oxide-Semiconductor) memory cells [77].

Since then, an intensive research on floating-gate non-volatile memories has been carried out to enhance their performance (i.e., high speed, high density and low power consumption) and to reduce the production costs. At the moment, flash memory is the fastest growing segment of the memory market and therefore receives enormous attention. In current flash memory technology, the gate dielectrics thicknesses (both tunnelling and blocking) are hardly scalable. As a consequence, the operating voltages of flash memories can not be reduced significantly below their current level.

These hindrances stimulate a continuous research on new cell designs and IC architecture. As will be shown further in this chapter, the replacement of the conventional floating gate with a layer of silicon nanodots together with implementation of the dielectric layers formed at low temperatures (see Chapter 3) enables the realization of the non-volatile memory cells with noticeably reduced thermal budget during the processing. This is opening an opportunity to integrate the memory cell arrays in the third dimension.

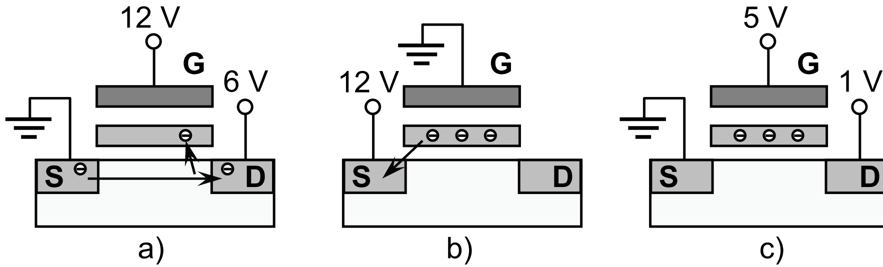


Figure 5.3: Example of flash memory with continuous floating gate (a) program, (b) erase and (c) read operations.

5.2.1 Memory cell operation principle

The operational principle of the flash memory is based on the charge storage in the floating gate (functioning as a charge trapping layer) of a MOSFET (shown in Figure 5.3), inducing a modulation of the device threshold voltage. The programming or erasing steps are realized by applying appropriate voltages to the control gate, source, and drain, so that the charge carriers can tunnel through the tunnelling oxide toward or away from the floating gate (Figure 5.3a,b).

After programming, the charge stored in the floating gate causes a threshold voltage shift equal to [78]:

$$\Delta V_T = \frac{Q_T}{\varepsilon_i} d_i \tag{5.1}$$

where d_i is the thickness and ε_i is the dielectric constant of the blocking oxide (see Figure 5.2) and Q_T is the charge per unit area.

The read-out of a flash memory is done by applying the gate voltage V_read with a value between the two possible threshold voltages and measuring the drain current. As shown in Figure 5.4, in one state the transistor is conducting current (state “1”), while, in another, the transistor is in cut off (state “0”). If the power supply is interrupted, the stored charge will remain trapped in the floating gate providing a non-volatility of the memory cell.

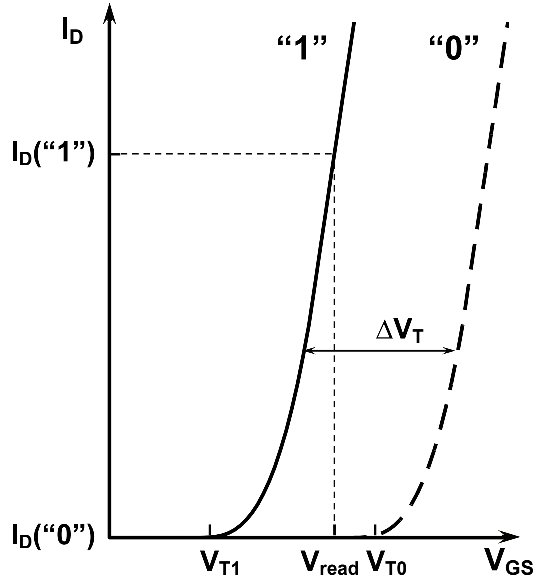


Figure 5.4: I-V Curves of the non volatile memory cell in "1" erased state and "0" programmed state.

5.2.2 Tunnelling mechanisms

During the programming and erasing steps two different mechanisms can be used to transport the charge carriers through the tunnelling dielectric (i.e. across the potential barrier): hot electron injection and Fowler-Nordheim tunnelling [78].

At large applied drain biases, the induced large electric field in the channel of an NMOS transistor is used to provide electrons with sufficient energy (i.e. hot electrons) to get over the barrier into the conduction band of the dielectric (shown in Figure 5.5a). This mechanism is called "hot electron injection" and is widely used for programming of the memory cells. However, the required high drain and gate voltages result in very high currents and therefore make the programming process extremely power consuming. Another disadvantage of the shown tunnelling mechanism is that it can be applied only for programming and not for erasing of the cell.

When a low (read) voltage is applied to the gate of the MOS transistor the shape of the energy barrier across the tunnelling oxide is trapezoidal. It is possible for electrons to tunnel through such a barrier directly to the conduction band of the next electrode (shown in Figure 5.5b). However, to ensure good retention characteristics of the memory cell the leakage current across the tunnelling oxide ideally should be equal to zero. Therefore, due to the reliability concerns in memory devices this type of tunnelling has to be negligible to provide the low leakage currents.

In case of high (program/erase) gate voltages, high leakage currents across the tunnelling oxide are required. When the effective barrier has a triangular shape, being narrower than the thickness of the tunnelling oxide, Fowler-Nordheim tunnelling can occur. In this case, electrons tunnel to the conduction band of the dielectric (as shown in Figure 5.5c). In order to provide fast programming and erasing steps it is required to apply a high electric field (in the range of 10 MV/cm) to ensure the Fowler-Nordheim tunnelling through silicon oxide. The strong advantage of this tunnelling mechanism is its low power consumption. This makes it possible to simultaneously erase large memory array blocks – the main merit of the flash memory.

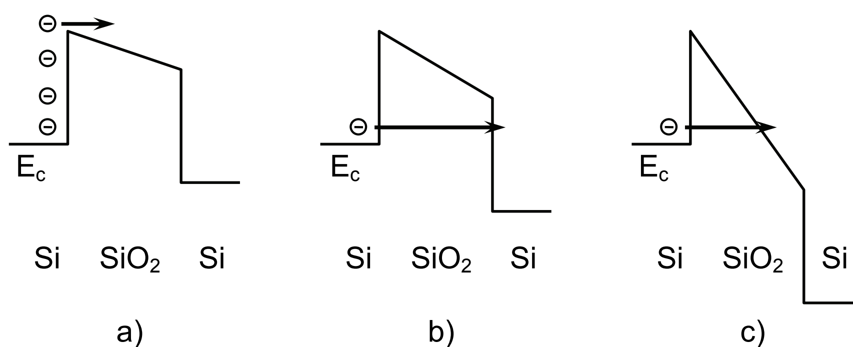


Figure 5.5: Energy diagram of the conduction band during hot electron injection (a), direct tunnelling (b) and Fowler-Nordheim tunnelling (c).

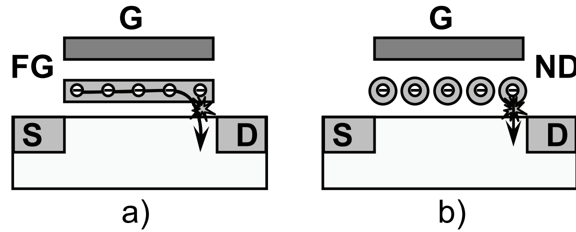


Figure 5.6: Possible leakage path in the tunnel oxide in a non-volatile memory cell with a continuous floating gate (a) and with nanodots (b). Once the continuous FG is shorted due to a defect in the tunnel oxide it can drain all stored (programmed) charge out from the FG. In a discontinuous FG the charge state is much less dependent on local leaks in the gate oxide which will discharge only a single nanodot isolated from others. That will reduce the impact of defects present in low-temperature dielectrics.

5.2.3 Memories with discrete floating gate

In this work an approach to fabricate silicon-nanodot memory cells with a low thermal budget (below 425 °C) is investigated. In this perspective, the advantage of the discontinuous nanodot floating gate over continuous floating gates is that the charge state is much less dependent on local leaks in the gate oxide (see Figure 5.6). This allows the use of CVD gate oxides with a higher density of weak spots compared to thermally grown oxide.

The major benefits provided by the use of a discrete floating gate are the increase of the memory's retention time, an ability to scale the tunnelling oxide thickness, a minimized drain-to-floating-gate coupling and perspective to realize multi-bit storage devices [37]. Additionally, the possibility to fabricate memory cells on re-crystallized amorphous-silicon layers, keeping thereby the total thermal budget of the process low, opens the way to 3-D memory structures inside the microchip's backend.

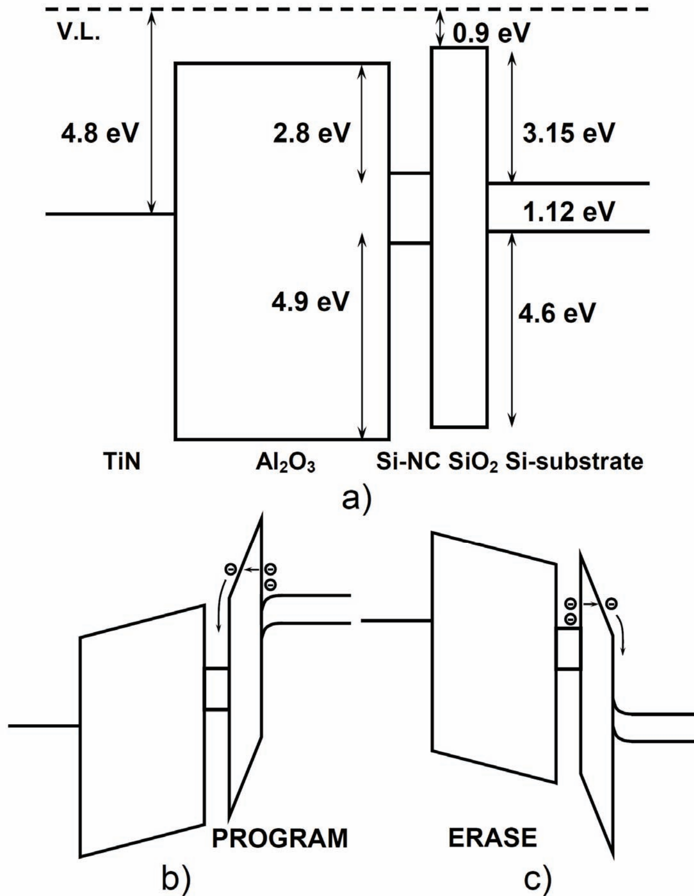


Figure 5.7: Energy band diagrams of multilayer structure with encapsulated Si-nanocrystals under flatband condition (a), during programming (b) and erasing (c) cycles. Si-nanodots have an increased band gap compared to bulk Si [79].

5.3 Memory cell characterization

In this work, the functional multilayer Al/TiN/Al_2O_3/Si-ND/SiO_2/Si stack (shown in Figure 3.2) was realized according to the process flow described in subchapter 3.2. As already mentioned, two different materials were chosen for the tunnel and blocking gate dielectrics (i.e. silicon dioxide

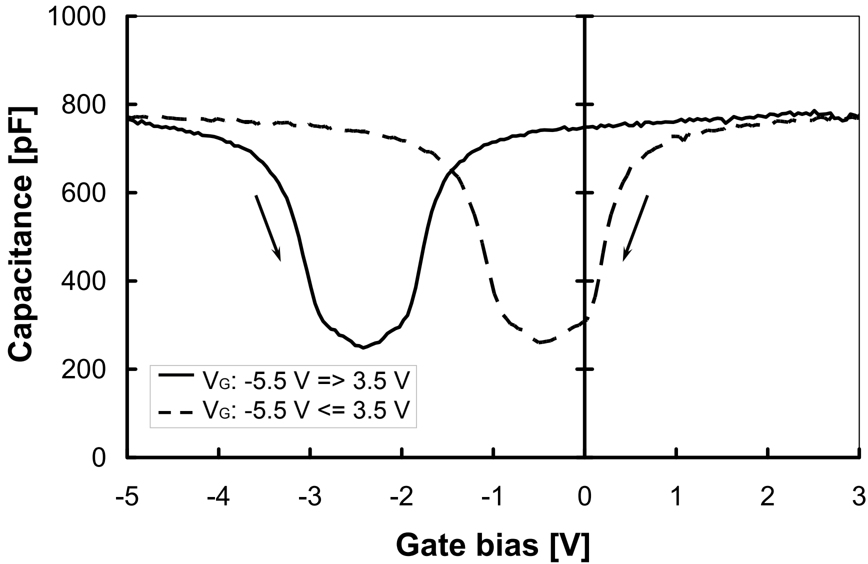


Figure 5.8: Quasi-static C-V hysteresis curves obtained during programming and erasing cycles for MOS structures with encapsulated silicon nanocrystals. Applied gate-substrate voltages: $V_{G\,prog} = 3.5\ V$ *and* $V_{G\,erase} = -5.5\ V$.

with $k = 3.9$ and alumina with $k = 9$, respectively), providing an energy band structure required for Fowler-Nordheim tunnelling through the tunnel oxide.

Figure 5.7a shows a schematic energy band diagram of the realized multilayer structure under flat band conditions according to [39, 80]. The encapsulated silicon nanocrystals are expected to act as charge trapping centres. During programming and erasing cycles due to the different dielectric material of tunnel and blocking oxides there is a much higher electric field induced across the thin SiO_2 film (see Figure 5.7b-c). That ensures the Fowler-Nordheim tunnelling mechanism to dominate during the charge carrier transport between the substrate and the nanocrystals, and at the same time prevents tunnelling through the blocking oxide.

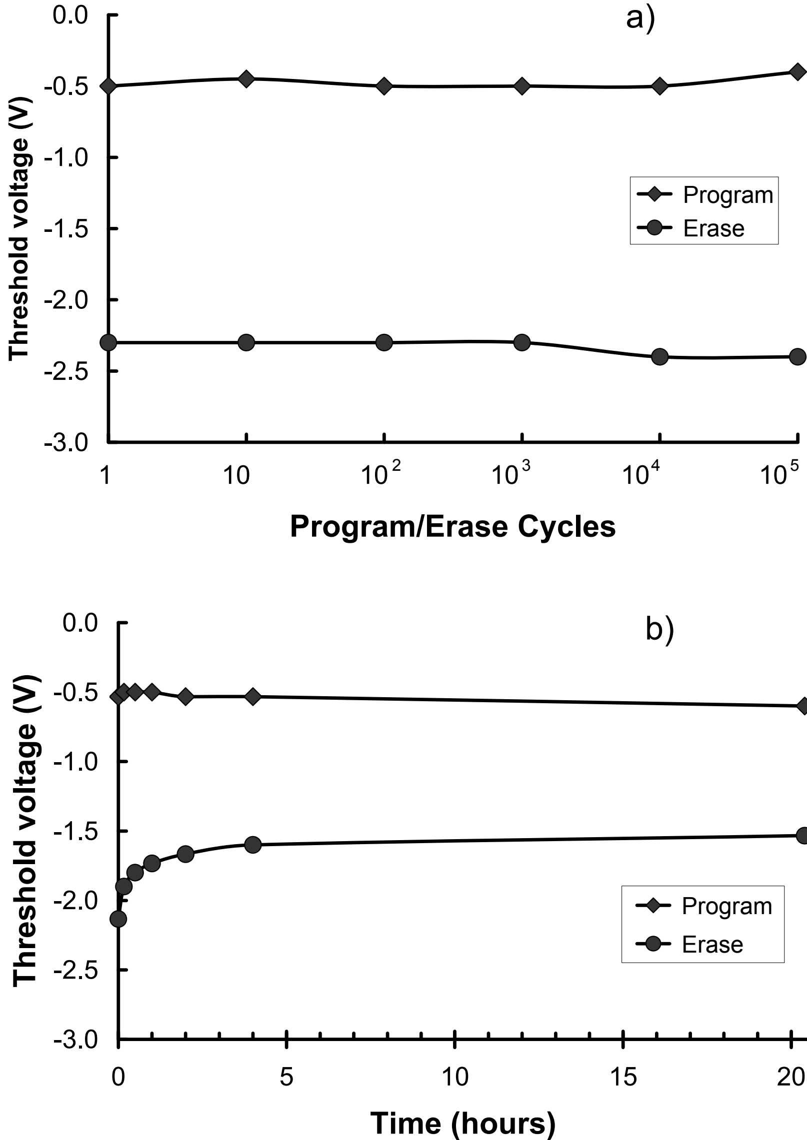


Figure 5.9: Endurance (a) and retention (b) measurements of MOS structures with encapsulated silicon nanocrystals

As charge is stored in the nanocrystals, i.e. between the substrate and the control gate, it dramatically influences the *C-V* characteristics of the

MOS capacitors. Figure 5.8 shows typical hysteresis curves observed during the quasi-static *C-V* measurements of the circular (500 µm in diameter) MOS capacitors with embedded nanocrystals. The width of the hysteresis corresponds to the threshold voltage shift (ΔV_T). Herewith, it can be concluded that the capacitors work as a memory cell.

To characterize programming and erasing behaviour of the multilayer structure, the endurance (Figure 5.9a) and retention (Figure 5.9b) of the above mentioned MOS capacitors were tested. The test devices were programmed by biasing the gate at $V_{G\,prog} = 3.5$ V and erased by biasing the gate at $V_{G\,erase} = -5.5$ V. Figure 5.9a shows a good endurance after 10^5 program/erase cycles, meeting basic flash memory cell requirements.

As it can be seen from Figure 5.9b during the first hour there is a significant change in the erase state. The reduction of the threshold voltage shift can be explained by discharging the slow states near the interface between the Si-substrate and the SiO_2 layer, and is not related to charge leakage from silicon nanocrystals. The charge trapped at the nanocrystals is retained. Hence, the realized non-volatile memory cells show a data-retention time longer than 20 hours.

5.4 Silicon nanodots for photonic application

The prospective implementation of optical data transfer within IC's requires efficient, CMOS-compatible light sources [81]. The integration of light emitting devices further demands process flows with very low thermal budgets, in order to prevent thermal degradation of the underlying device layers. Silicon based light emitters have the potential to meet these process requirements, but often emit light with low quantum efficiency due to the indirect band gap of silicon. Moreover, light emission in bulk silicon-based devices is constrained in wavelength to infrared emission.

A possible solution to overcome the described drawbacks of silicon photonics is to make use of quantum-confined excitonic emission in silicon nanodots [59, 60, 82]. An enhanced emission can be obtained from silicon nanocrystals in comparison to bulk silicon [83-85]. However, the problem of

sufficient size control in combination with low-temperature CMOS back-end compatible processing needs further investigation.

Optically active functional multilayer Al_2O_3/Si-ND/../Si-ND/Al_2O_3 stacks (shown in Figure 3.3) consisting of four layers of silicon nanodots embedded in an alumina matrix were realized at low temperatures (300-325 °C) according to the process flow described in subchapter 3.3. The encapsulating Al_2O_3-matrix, realized without vacuum break, provided a sufficient protection against further oxidation of the Si-ND layers during the next processing steps. The size of silicon nanodots was determined by their deposition parameters, eliminating any need for further high temperature processing steps.

5.4.1 Photoluminescence and electroluminescence

The photoluminescence of layers containing silicon nanocrystals with different thicknesses/sizes (i.e., deposited during 10, 20 or 30 min from trisilane at 300 °C) was investigated (as described in subsection 2.5). The measured spectra show broad peaks centred at approximately 800 nm, 840 nm and 870 nm for 1.6 nm-, 2.2 nm- and 3.5 nm-thick Si-ND layers, respectively. A “blue-shift” is observed with decreasing the layer thickness (shown in Figure 5.10). However, the magnitude of the shift is not correlating with the calculations performed for excitonic recombination [86]. The PL emission maximum for 1.6 nm-large Si nanodots is expected to be in UV range due to the band-gap widening caused by the quantum confinement effect.

One has to bear in mind that at the interface between Si-ND and alumina matrix Si=O bonds are formed during the initial stage of Al_2O_3 deposition, when the wafer was exposed to H_2O. Such Si-ND surface passivation introduces a new recombination mechanism, playing a significant role especially when the nanodot size is smaller than 3 nm. The Si=O bonds generate new energy states lying inside of the widened band gap. The recombination of the trapped excitons (i.e. electrons and holes

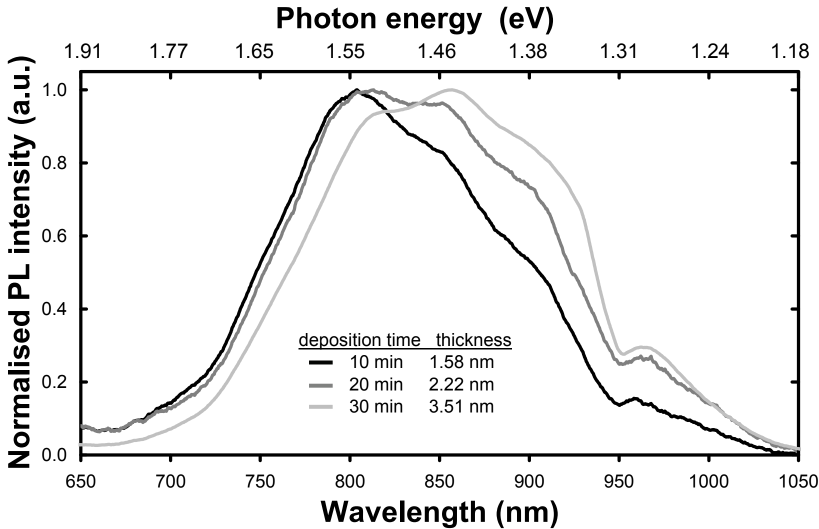


Figure 5.10: Photoluminescence spectra measured for layers with different thicknesses (excited using the 488 nm line of an Ar^+ laser).

trapped on the Si=O bond) becomes dominant, precluding further "blue-shift" of the PL spectra maximum [82].

We can conclude that the photoluminescence is presumably attributed to exciton recombination in large silicon nanodots (∅ > 3 nm) and in associated oxygen related surface states in small ones (∅ < 3 nm) [87].

An additional quasi-peak at 965 nm is attributed to the luminescence from bulk silicon which is not registered at the higher wavelengths due to the non-responding of the CCD detector at these wavelengths (see Figure 2.8).

The multilayer stack containing 3.5 nm-thick Si-NC layers in alumina matrix was further annealed in forming gas (10% H_2:N_2) at 500 °C for 10 minutes. This resulted in an increase in the photoluminescence spectra maximum of up to 400% of the initial intensity, as shown in Figure 5.11. The quantum efficiency for silicon nanodots in alumina is estimated to be about 0.3% [34].

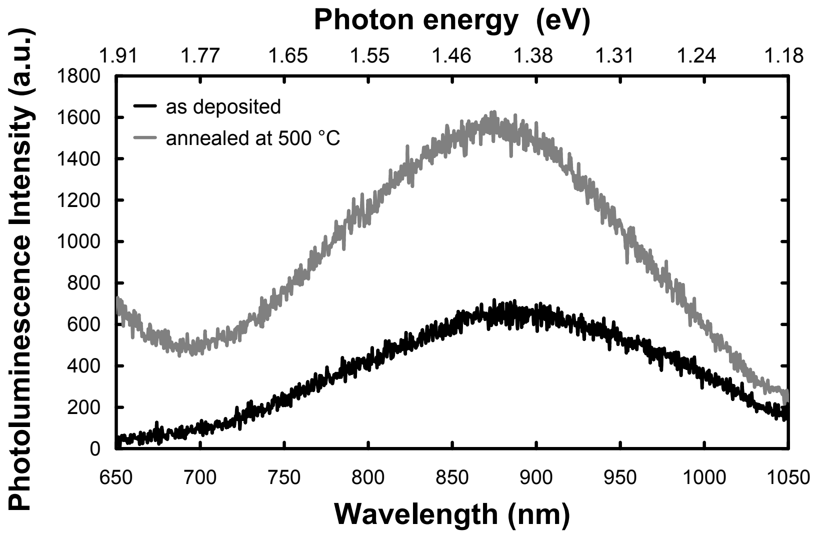


Figure 5.11: Photoluminescence spectra showing the enhancement of the luminescence after annealing in forming (H_2 + N_2) gas atmosphere.

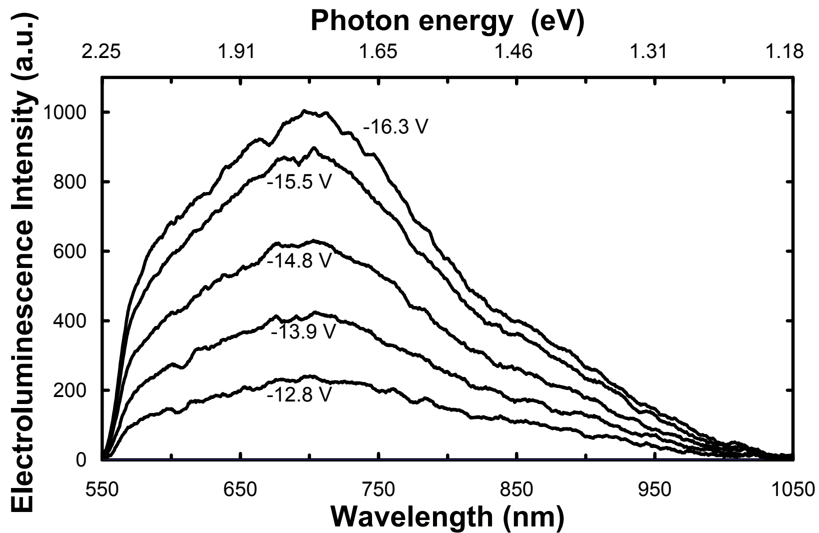


Figure 5.12: Electroluminescence spectrum at various biasing conditions.

The electroluminescence from the silicon nanocrystals was measured on the metal-insulator-semiconductor capacitor structures. A schematic measurement set-up is described in subsection 2.5 and shown in Figure 2.9. The sample with the top contact on alumina was negatively biased with respect to the contact on the silicon substrate site. The electroluminescence spectrum was measured at various biasing conditions, and is shown in Figure 5.12. The mechanism of electroluminescence is most probably the impact ionization by hot electrons [87]. A slight shift of electroluminescence maximum was observed in comparison to the photoluminescence spectrum which can be due to the different excitation mechanism.

A decrease in the emission intensity over time was registered during electroluminescence measurements. This can be attributed to the damage in the alumina matrix caused by the tunnelling currents.

5.5 Conclusions

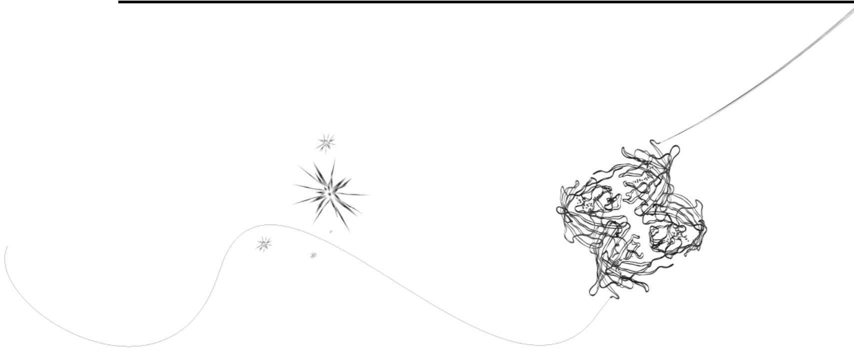
Functional multilayer stacks with embedded silicon nanodots were used to fabricate non volatile memory cells and light emitting structures. Good program and erase behaviour of memory devices is demonstrated. The described floating-gate stack module can be combined with low-temperature laser crystallized silicon resulting in a wide range of emerging technologies, such as 3-D integration.

The demonstrated optical activity (i.e. photoluminescence and electroluminescence) of the structures with silicon nanodots can lead to their further integration into silicon-based IC’s using the low-temperature CMOS post-processing technology.

"We don't know who discovered water,
but we know it wasn't the fish."

Marshall McLuhan

6 Laser crystallization of amorphous silicon



6.1 Introduction

The thin-film transistor (TFT), realized in the earlier ’60s [88] and based on the concept already patented in the ‘30s by J. Lilienfeld [89, 90] and O. Heil [91], is a basic element in today’s integrated circuits. In addition to the primarily used CdS as the active material, a wide range of materials has been investigated (i.e., CdSe, Te, InSb, polysilicon, amorphous silicon and germanium).

In the ’70s, a growing demand on large-area low-cost electronics for liquid crystal displays (LCDs) stimulated intensive research on CdSe and a-Si as promising active materials for TFTs. In 1979, LeComber et al. demonstrated the first functional a-Si field-effect transistor suitable for application in LCDs [92]. Thereby, an era of amorphous silicon domination in the large-area TFTs marked was started. But low mobility of electrons resulting in a low device speed, remained a large drawback in a-Si TFTs.

Since 1990, organic-based semiconductor active layers with electron mobilities similar to that of *a*-Si are considered as a promising alternative especially for the electronics on flexible plastic substrates. However, the low mobility typical for the above-mentioned materials makes this technology unfeasible for realization of drive circuits integrated within the active matrix level.

Another problem appearing nowadays, is that integrated circuit downsizing is approaching its physical and commercial limitations. Therefore, a 3-D integration is gaining attention. One pursued route for three–dimensional integrated circuits is the stacking of several active layers by subsequent thin-film depositions (i.e. monolithic 3-D integration). This approach demands low thermal budgets [3, 4, 7, 93] in combination with good quality semiconductor and dielectric films.

The metal chalcogenide compounds, as an example of alternative materials for TFT application, become very attractive due to the higher mobility and increased device stability. Reported in [94] spin-coated chalcogenide SnS_2 or $SnSe_2$ thin films impress additionally with their high

uniformity at very low thicknesses in combination with the simple deposition technique. However, the fabrication chemistry is hardly CMOS compatible and scarcely suitable for high throughput, what limits their application also in large-area electronics [95].

The application of polycrystalline silicon TFT's with their superior mobilities enables successful integration in case of active matrix-addressed flat-panel liquid crystal displays and 3-D ICs. While aiming at low thermal budgets during processing, the thin-film transistor technology where the polysilicon active layer is formed through laser crystallization of low-temperature deposited amorphous silicon [96-101] offers just that. However, the quality of the crystallized film depends on a number of parameters, e.g., film thickness, laser wavelength, laser energy density, laser repetition rate and pulse duration.

A large number of gas and solid state lasers has been used for processing of silicon. The available systems provide wavelengths from 193-308 nm for excimer lasers and up to 1064 nm for Nd:YAG laser. The laser choice is dictated by certain conditions. In case of 3-D integration the interlayer oxide must be transparent at this wavelength to prevent its heating to avoid cracks, deformation and other damage [102]. At the same time, the absorption coefficient for the amorphous Si film must be high enough to provide complete melting of the irradiated film.

In the case of excimer laser crystallization (308-nm wavelength), the laser beam penetration depth into the amorphous silicon and polysilicon extracted from the spectroscopic ellipsometer measurements [103] is < 10 nm, so primarily, the thin top layer of the silicon film is melted and only further heat diffusion provides a complete melting of the film. For this reason we chose for an irradiation at 515 nm wavelength, which has a much lower measured absorption coefficients. This ensures a larger penetration depth of ≈ 49 nm for a-Si and near 200 nm for the crystallized poly-Si film [103], leading to a more homogeneous melting of the silicon layer [102] [104, 105]. This widens the process window for the re-crystallization in terms of the laser power and pulse duration [104-106]. Additionally, the use

of the green laser reduces the maintenance expenses and assures a higher safety processing conditions [107].

With this chapter a novel approach to control the location of the grain boundaries during the laser crystallization is introduced. It requires only one additional mask and uses only process steps already available in the process flow (i.e., no additional deposition equipment is required), being therefore CMOS compatible. The results of surface and texture analysis of the crystallized silicon films with preformed a-Si lines are presented and discussed. The next section is devoted to the sheet resistance measurements used to investigate an anisotropic nature of the obtained film and to approve a high efficiency of the green-laser-anneal for the dopant activation (i.e., arsenic and boron). In the next section, the method to measure the surface and volume recombination in the crystallised films is introduced.

Consequently, large-grain p- and n-channel TFTs on polysilicon stripes realised with Al_2O_3- and SiO_2-gate dielectrics are presented, and their location-dependent electrical performance is discussed. The last section of this chapter deals with CMOS integrated circuits (i.e., inverters and ring oscillators) realised at low temperatures on crystallized polysilicon stripes and their characterization.

6.2 Green-Laser Crystallization

6.2.1 Crystallization of uniform silicon films

During pulsed laser annealing of the homogeneous amorphous silicon film the applied laser energy density has to be accurately adjusted with respect to the film thickness, to provide an optimal re-crystallization process (i.e. formation of the large grain polysilicon film). Figure 6.1 schematically shows three general regimes observed in thermally treated films.

At low laser energy densities only a top layer of silicon film melts - so called partial melting regime (Figure 6.1a). Due to the large difference in melting temperatures for amorphous ($T_a \sim 1420$ K) and crystalline silicon ($T_{cl} \sim 1685$ K) [108], the molten layer is deeply undercooled. The vertical solidification starts from the bottom of the molten region yielding fine grain

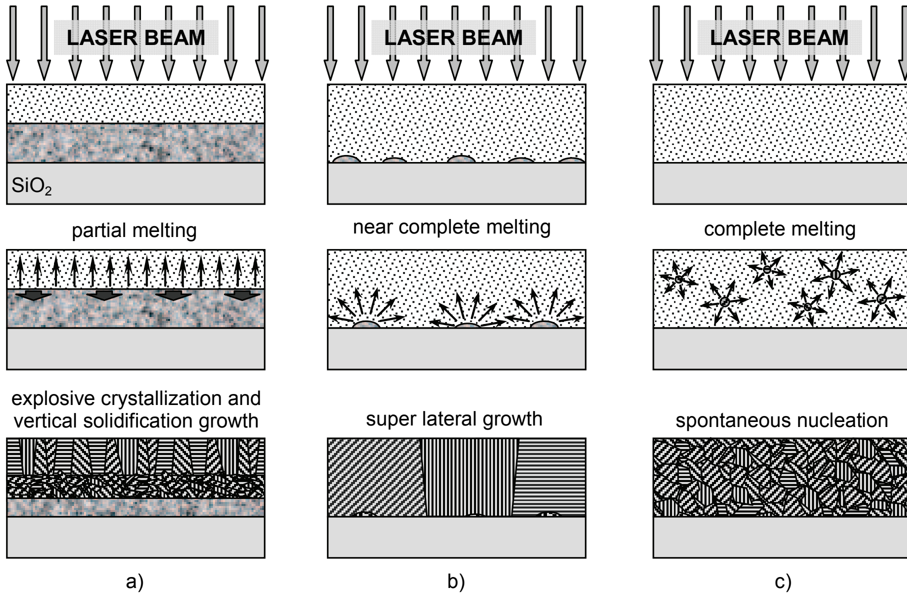


Figure 6.1: Partial melting (a), near complete melting (b) and complete melting (c) of silicon film.

poly-Si with a columnar structure [109]. The heat, released during the solidification, increases the temperature of the re-crystallized poly-Si over T_a, therefore the underlying a-Si starts to melt. Being strongly undercooled this thin molten layer is immediately crystallized into the fine-grain poly-silicon. The subsequent heat release maintains the self-propagating melting front, which moves deeper into the underlying amorphous silicon at velocities of 10-20 m/s [110]. This crystallization phenomenon is called explosive crystallization [111, 112]. As a result, the crystallized film consists of a large-grained polycrystalline top layer and a fine-grained poly-Si layer, lying beneath (shown in Figure 6.1a). Additionally, a part of the amorphous material could remain at the bottom if the explosive crystallization does not reach the oxide interface.

In the case of the complete melting regime (shown in Figure 6.1c), the laser fluence is high enough to melt the amorphous Si film completely. In this case, due to the absence of nucleation centres the molten film becomes

deeply undercooled. Therefore, the subsequent crystallization is determined by the extensive spontaneous nucleation within the total volume of the undercooled molten Si. The grain sizes obtained in this regime are very small (much below the film thickness), being typically in the order of tens of nanometres in diameter [113].

Besides these two regimes, a third one exists within a very narrow laser fluence range. At those laser energies the unmolten silicon film, remained underneath the molten material, is no longer a continuous layer, but consist of solid islands separated by molten regions (shown in Figure 6.1b). Therefore, this regime is also called the “near complete melting” regime [114, 115]. During the subsequent solidification the unmolten silicon islands act as crystallization seeds, inducing the lateral crystal growth, which propagates into the undercooled molten Si (also called “super lateral growth” regime). As a result, a polysilicon film with large grains is formed. The grain size in this case could amount to several multiples of the film thickness [96].

The large crystalline regions obtained during super lateral growth are attractive for TFT technology because of the significantly less number of the defects attributed to the grain boundaries, subsequently leading to the enhanced thin film electronic device performance. However, to achieve the conditions required for super lateral growth across large silicon film areas, many parameters should be controlled very precisely (i.e. laser energy density and beam profile, film thickness etc.). Otherwise, minor variations lead to partial- or complete-melting regimes, with consequent formation of fine-grained film as described above.

Based on controlled manipulation of the super lateral growth regime several techniques aiming sequential lateral solidification (i.e. directionally solidified microstructures with unrestricted length) are developed [116, 117].

Another issue with laser-crystallized uniform silicon films is the grain size and the random position of grain boundaries. They result in randomly distributed electrical potential barriers, leading to large device-to-device variations, especially when the device size is comparable with the grain size. Therefore, to reduce the technological complications and increase the

predictability of the film properties, the laser crystallization process needs to be improved.

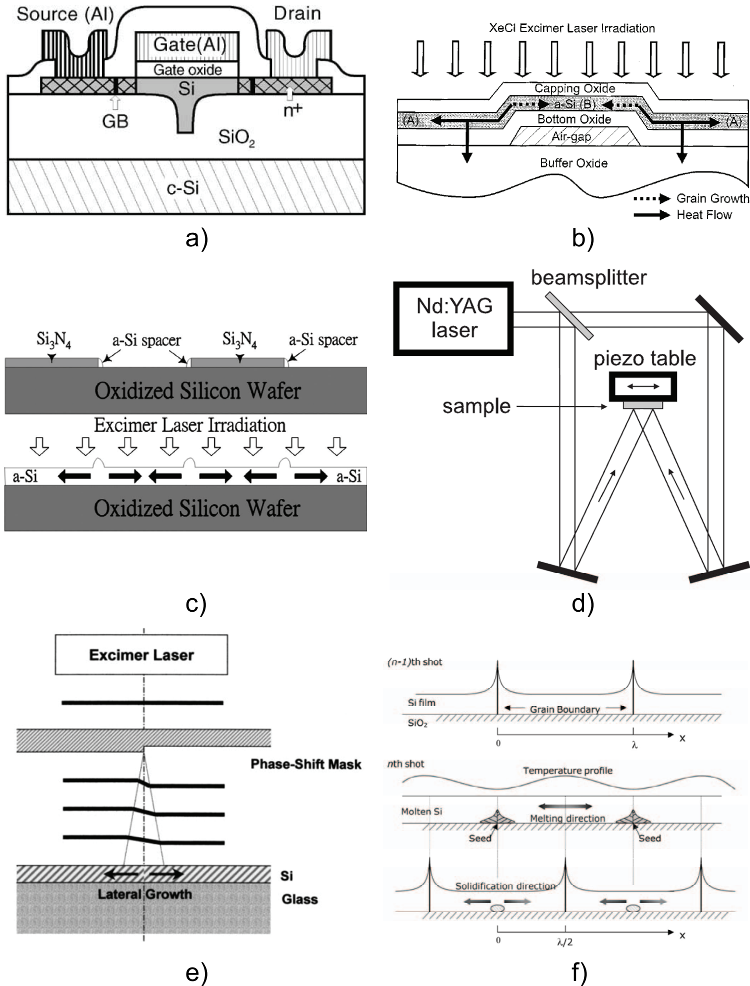


Figure 6.2: Grain boundaries location control techniques: μ-Czochralski (grain-filter) process [118] (a); floating active structure with air-gap formation [119] (b); amorphous silicon spacer structures [120] (c); pulsed interference laser crystallization [121] (d); phase-modulated excimer laser annealing [122] (e); laser-induced periodic surface structures [123] (f).

6.2.2 Grain boundary location control approach

To obtain a long-grained polysilicon film as a result of super lateral growth and to maintain the control over the location of the grain boundaries, additional modifications of the laser beam or the initial silicon film are required.

Recently, several techniques (shown in Figure 6.2a-c) were reported to lithographically control the position of grain boundaries in excimer laser crystallized silicon films: through buried crystallization seeds (introduced in 2001) [118], two-pass laser crystallization (2001) [124], air-gap formation (2002) [119] or the introduction of silicon spacers (2005) [120]. In all cases, dedicated new process steps are added to the process flow.

Alternatively, laser beam intensity modulation methods (shown in Figure 6.2d-f) like pulsed interference laser crystallization (1998) [121], phase-modulated excimer laser (PMELA) annealing (2001) [122] or LIPSS technique (coming from laser-induced periodic surface structures) (2006) [123, 125] are providing partial control over the location of the grain boundaries. It has to be mentioned that techniques shown in Figure 6.2b-e are classified as 1-D location control methods (due to ability to control the position of grain boundaries in one direction and trying to minimize the number of grains in other direction), while the technique shown in Figure 6.2a ensures 2-D grain location control with a great positioning accuracy. Bearing manufacturing cost and yield considerations in mind, it is at this time unclear which is the most effective solution for controlled grain formation.

To induce a desired orientation in crystallized silicon films, a technique called graphoepitaxy, has been proposed [126-129]. In this method, the appropriate surface relief gratings etched into SiO_2 substrates are used to create textured poly-silicon film with predicted uniform orientation. However, aiming vertical solidification, graphoepitaxy does not provide any control over the location of the grain boundaries. Due to a low spatial period of gratings and high angle accuracy in “saw-tooth” structures, the expected large manufacturing costs might be the main drawback of this method.

Following the sequential lateral solidification approaches using spacers and seeds, we recently proposed a new approach to control the location of grain boundaries [30-32], as illustrated in Figure 6.3. An amorphous silicon layer (with typical thickness 50-100 nm common for poly-Si TFTs [130]) is deposited over parallel amorphous silicon lines, oriented in the laser-crystallization direction. During laser annealing a lateral temperature gradient in the molten silicon will result. Re-crystallization will start from the coolest (thickest) positions, and ends in between two lines where the random crystal boundary will form. Thus, long crystals aligned in one direction will be formed.

In the shown method only one additional lithography step is added. Moreover, all the used process steps are already present in the standard process flow used in CMOS manufacturing. This fact makes the described approach very attractive (from technological and commercial point of view) for its further implementation in 3-D integration of ICs.

6.2.3 Crystallization of preformed silicon films

On 100 mm, 5-10 Ω·cm Si wafers thermally oxidized to grow a 0.9 μm SiO_2 layer, a 50 nm thick a-Si film was deposited by LPCVD (from SiH_4) at

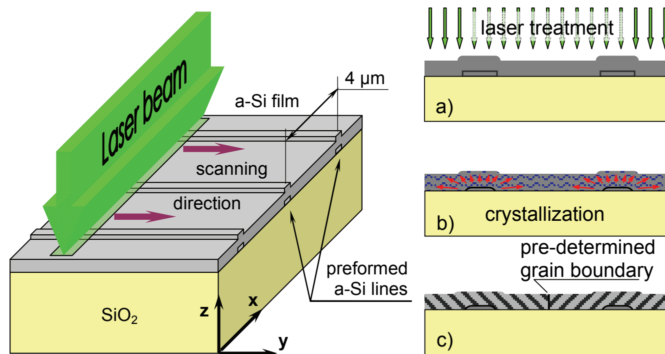


Figure 6.3: Crystallization process of a silicon film with preformed lines. Left: illustration of the crystallization step. Left: (a) laser treatment, melting the silicon film, (b) crystallization process – super lateral growth, (c) finally crystallized film with predefined grain boundaries.

550 °C, in which lines ~ 0.5 µm wide at a 4 micron distance were patterned using conventional lithography steps (mask aligner EVG 620). A second 100 nm a-Si layer was deposited with the same LPCVD process, resulting in an amorphous film with a periodically varied thickness (Figure 6.4).

The film was then crystallized using the laser optical system LAVA at INNOVAVENT GmbH, utilizing a green laser emitting at 515 nm with specifications described in Section 2.3.

The applied beam length was 8 mm and the width was 5.8 µm, both Full-Width Half-Maximum (FWHM) values. The pulse duration was 206 ns at repetition rate of 50 kHz. The scan velocity was 5.68 mm/second providing a beam overlap of 98 %. Silicon film crystallization was investigated at laser energy densities ranging from 0.6 J/cm^2 to 1.2 J/cm^2.

During the laser crystallization, the periodically varied thickness locally results in non-molten lines deeply embedded in the molten silicon. These solid regions influence the temperature gradient in the lateral direction perpendicular to the laser scan direction and serve as the crystallization centres for super lateral crystal growth (see Figure 6.3a-c). The thicker film regions crystallize first, followed by crystallization of the remaining thinner regions. Thereby the dominant crystal orientation can laterally extend to the

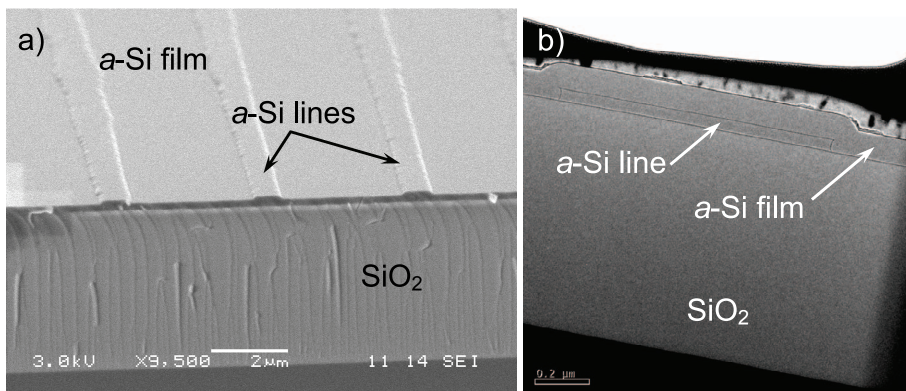


Figure 6.4: SEM (a) and TEM (b) cross-section image of amorphous silicon film with a periodically varied thickness.

grain boundaries, with a possible formation of intragranular ridges and hillocks [131].

6.2.4 Surface and texture analysis of crystallized films

As could be seen from analysis with AFM (see Figure 6.5), the surface of the silicon film even at optimum process conditions was not completely smoothed during laser crystallization. The crystallized film still exhibited a periodical height variation, remnant of the initial pre-formed lines. Therefore, for instance film planarization (e.g. using chemical-mechanical polishing) may reduce the deterioration effects in manufactured devices induced by this surface. In this research the planarization was not carried out.

An important parameter for the crystallization process was the choice of line width and line pitch. At 4 μm pitch and 0.5 μm line width we obtain the largest-width grains. If we increase the line pitch above 4 μm the grains do not extend wide enough perpendicularly to the laser scan direction. If the line width is larger than 0.5 μm the topography after crystallization is considerable – only thin lines are partly planarized during the crystallization

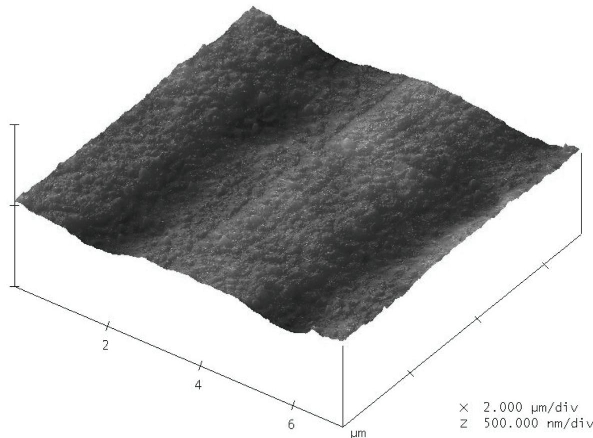


Figure 6.5: AFM image of crystallized Si film morphology (overall roughness RMS = 24.2 nm; local roughness RMS = 8.6 nm).

step. A thicker buried silicon line also leads to undesirable topography. The reduction of the line thickness below 50 nm leads to process window narrowing.

To gain continuous super lateral crystal growth starting from the crystallization centres on the bottom of the molten silicon it is important to have no oxide layer formed between the lines and the upper (second) layer of silicon. This can be achieved by immediate a-Si deposition on a hydrogen terminated Si-surface formed after the last HF dip during stripe patterning. Figure 6.6a shows the cross-section of the crystallized silicon film with the grain propagated from the silicon line into the film lying above. An interruption of the super lateral crystal growth is shown on Figure 6.6b-c.

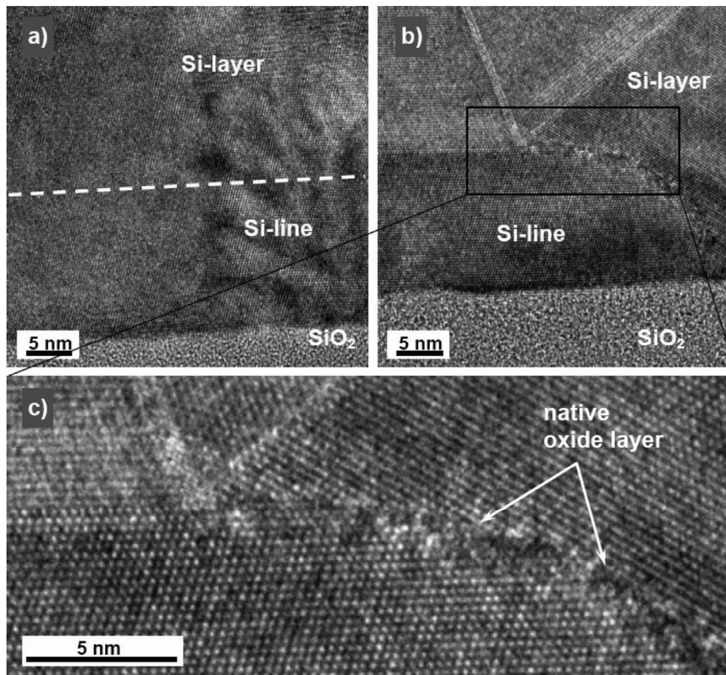


Figure 6.6: TEM images of crystallized silicon films: (a) super lateral crystal growth and (b) fine grain formation on the Si-line and the Si-layer interface (native oxide layer between Si-line and Si-layer is enlarged in (c)). The dashed line indicates the location of interface between the Si-line and -layer.

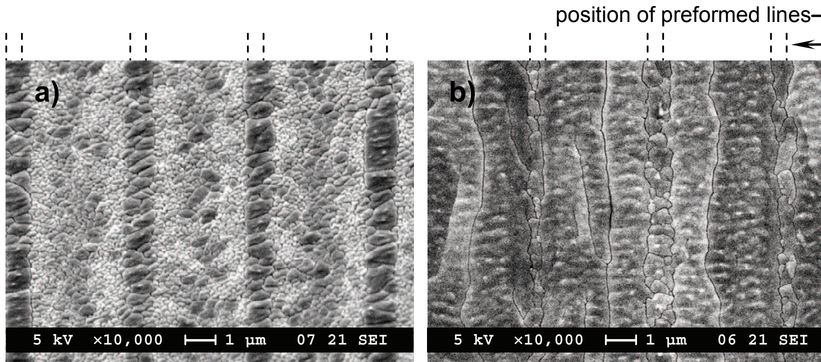


Figure 6.7: SEM images (after Wright etch) of a-Si films crystallized with energy densities 0.6 J/cm² (a) and 1.0 J/cm² (b) at 98% laser beam overlap.

Here, the presence of an interfacial layer (i.e., native oxide, which amount varies across the sample) on the silicon-lines separates the crystallization of the bottom and top layer resulting in the formation of smaller polysilicon grains.

The crystallinity of the silicon films is visualized by Wright etching as shown in Figure 6.7a-b. At sufficiently high laser energy, the material forms long crystalline stripes. This is confirmed by electron backscatter diffraction (EBSD) analysis (see Figure 6.8). The electrically active random grain boundaries (marked with black in Figure 6.8a) [132-134] in the films crystallized with 1.0 J/cm² are oriented mostly parallel to the preformed a-Si lines, i.e., in the laser scanning direction, providing a good control over their location (see Figure 6.7b and Figure 6.8). The grain boundaries oriented perpendicular to the laser scanning direction (marked with yellow in Figure 6.8a) mainly are electrically less active twin boundaries (with $\Sigma=3$) formed during the lateral growth to release thermal stress in crystallized film [135-137]. The concept of enlarged crystalline grains formation is therefore proven. Based on Figure 6.7b and Figure 6.8a we can make a rough estimation about the number of grain boundaries per device channel length (~ 0.2 twin grain boundaries/µm for parallel, and ~ 0.6 random grain boundaries/µm for perpendicular devices).

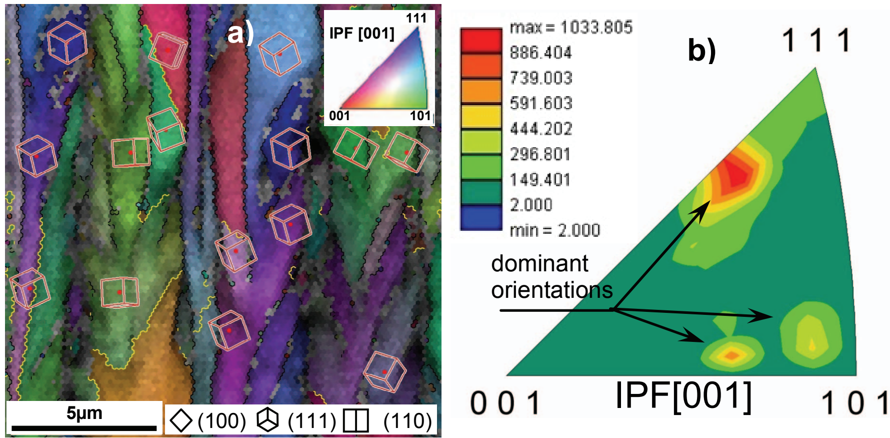


Figure 6.8: Crystal orientation map (a) and normal direction inverse pole figure (IPF) extracted from the orientation map (b) of crystallized silicon films (1.0 J/cm^2 at 98% laser beam overlap; the inset shows the colour key indicating the orientation aligned with the surface normal).

The irradiation with a lower energy (0.6 J/cm^2 at 98% overlap) resulted in insufficient film melting. This leads to a fine-grain structured silicon film (see Figure 6.7a).

Figure 6.8b shows the relative prevalence of certain grain orientations with respect to the film surface normal direction, observed by EBSD. The dominant orientation of examined sample is (112), with fractions of (102) and (142) oriented grains (due to limited statistics, more measurements are needed for definitive conclusions about the complete sample series).

It should be noted that the exact process window for laser crystallization may vary upon the layer stack underneath the *a*-Si film, because the thermal diffusion is different [138]. A silicon heat sink layer can alleviate this problem [139]. The silicon layer thickness is more than the absorption length for the used wavelength, in particular at higher temperatures. Therefore we expect that interference inside the silicon film can be neglected.

6.3 Sheet resistance ($R_\square$) measurements

The laser-crystallized large-grain poly-Si films offer better conduction properties than conventional poly-Si films as devices can be fabricated within a single grain. When the position of grain boundaries is random, it is rather difficult to realize devices with similar characteristics over large substrate areas. As the grain boundary location control is strongly improved by the use of preformed *a*-Si lines, higher conductivity and a decreased spread in the device performance can be expected.

Another important issue is the activation efficiency of the implanted boron and arsenic ions. During the continuous downscaling the channel resistance in TFTs decreases, however it is essential also to keep the parasitic source/drain (S/D) resistance at low levels to maintain the high on-current. Therefore, high activation levels are required after second laser treatment. The latter was confirmed by measuring the electrical sheet resistance of the laser annealed films.

6.3.1 Fabrication of long diffusion area test-structures

Due to the expected anisotropy in electrical behaviour, the conventional four-point method for measuring sheet resistance (e.g. van der Pauw or Greek cross) [140] could not be employed. Thus, sheet resistance was measured in both directions using Kelvin-contacted silicon stripes of 300 μm length and 5, 10, and 15 μm width (Figure 6.9), oriented in both the *parallel* (*y*-axis) and *perpendicular* (*x*-axis) current-flow direction with respect to the random grain boundaries.

The crystallized silicon films were initially patterned, to form stripes. Then, BF_2^+ (1×10^{15} cm^{-2}) and As^+ (4×10^{15} cm^{-2}) ions were implanted at 55 keV to form p- and n-type stripes. Arsenic was chosen instead of phosphorus because of the lower diffusion and smaller implantation depth at the same acceleration voltage. The higher solubility of arsenic allows an implantation of higher dose in comparison with boron.

The dopant activation was done by a laser optical system similar to that used for the crystallization (see Section 2.3). The applied laser energy

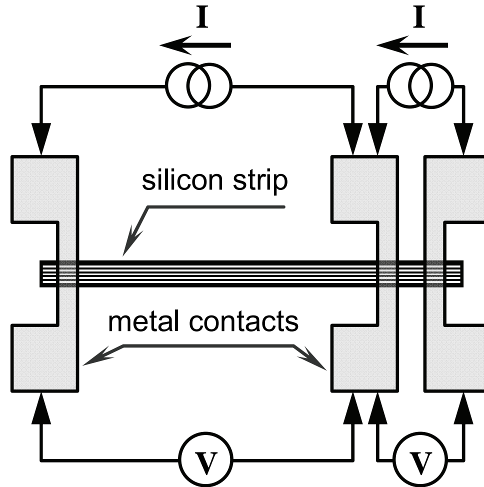


Figure 6.9: Measuring configuration for determining $R_{\square}$ (top view). The length ratio between the left and right part of the silicon strips on the same structure was 250 µm / 10 µm or 200 µm / 20 µm, and the width was 5, 10, and 15 µm.

density was 0.4 J/cm2; the beam length was 5.16 mm and the width was 28.4 µm. The pulse duration was 300 ns with a repetition rate of 10.2 kHz, and the scan velocity was 14.5 mm/second, providing a beam overlap of 95%. Under these conditions the dopant becomes active without silicon re-melting.

6.3.2 Sheet resistance of laser crystallized films

The sheet resistance was measured by means of long-diffusion area test structures (Figure 6.9), for both the *parallel* and *perpendicular* orientations of the silicon stripes with respect to the random grain boundaries. These resistivities, labelled ($R_{\square||}$) and ($R_{\square\perp}$) respectively, are shown in Figure 6.10. Clearly (and as expected) the sheet resistance is lower when current flows parallel to the random grain boundaries. Moreover, the spread of $R_{\square||}$ is significantly lower in comparison to the $R_{\square\perp}$ spread, for both p- and n-type films. In samples crystallized at 0.7 - 1.0 J/cm^2 laser energy densities, the

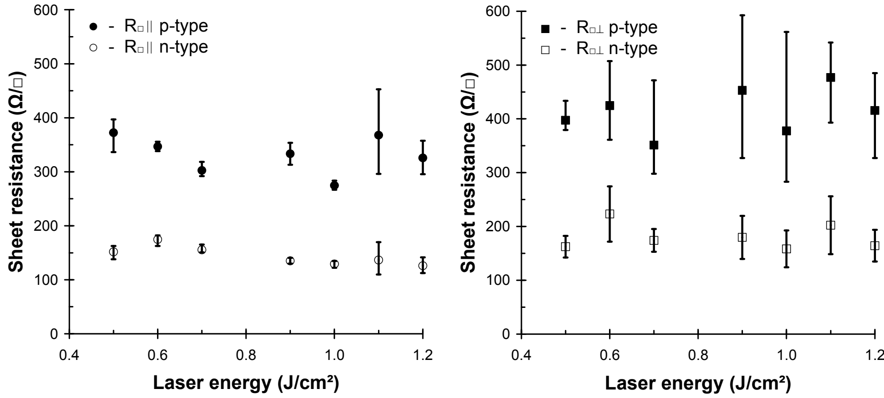


Figure 6.10: Sheet resistance spread of crystallized a-Si films versus laser crystallization energy for the test-devices oriented parallel (left) and perpendicular (right).

parallel sheet resistance of both films has an rms spread below 5 % in contrast to the perpendicular rms spread of up to 21 %. Furthermore, it is important to note that the mean sheet resistance values averaged over the entire crystallization energy range (0.5 - 1.2 J/cm^2) were also dependent on the current flow direction with respect to the grain boundary orientation. Namely, for n-type silicon film crystallized with 1.0 J/cm^2 and annealed afterwards with 0.4 J/cm^2, the average sheet resistance is 129 and 158 Ω/□ (i.e., 18 % difference) for parallel and perpendicular oriented islands, respectively. For p-type silicon film, the orientation dependence of the sheet resistance is even larger, being equal to 275 Ω/□ for parallel and 378 Ω/□ for perpendicular oriented islands (27 % difference). The figure further indicates that the laser energy dependence is weak, suggesting an appreciable process window.

From the calculated resistivity values ($\rho_{n,||}$ = 1.4 mΩcm for n-type and $\rho_{p,||}$ = 3.0 mΩcm for p-type silicon film) we can derive the concentrations of electrically activated donor and acceptor atoms, i.e., approximately 3×10^{20} cm^3 for arsenic and 8×10^{19} cm^3 for boron, near the saturation limit of heavily doped films [141]. This corresponds to an activation level above

Symbol	N-MOS		P-MOS	
	$R_{\square\parallel}$	$R_{\square\perp}$	$R_{\square\parallel}$	$R_{\square\perp}$
Average $R_{\square}$ (Ω/□)	129	158	275	378
Difference $R_{\square\parallel}/R_{\square\perp}$	18 %		27 %	
Activated dopant concentration (cm^{-3})	(As) 3×10^{20}		(B) 8×10^{19}	
Resistivity (mΩcm)	1.4		3.0	
Activation level	> 80 %		> 80 %	

Table 6.1: Characteristics of crystallized silicon films after implantation and laser dopant activation.

80 % for both impurities. The summarized film characteristics evaluated from the resistivity measurements are shown in Table 6.1.

6.4 Surface and volume recombination in crystallized thin films

The volume and surface recombination processes strongly influence the performance of SOI devices; in particular floating body effects, transient current and forward biased junction current can be affected [142, 143]. Therefore, recombination parameters (i.e., carrier recombination lifetime and surface recombination velocity) should be taken into account when designing MOSFET devices. The evaluation of these parameters allows drawing a conclusion about the effectiveness of the laser crystallisation processes.

6.4.1 Modelled recombination in p-i-n diode

Due to the poly-crystalline structure of the crystallized films, a significant volume recombination is expected in addition to the surface recombination. It is difficult to distinguish between the two recombination processes using a single measurement. However, measuring thin-film double-gated diodes by biasing independently front- and bottom-gates (shown in Figure 1.1) makes it possible to distinguish between the

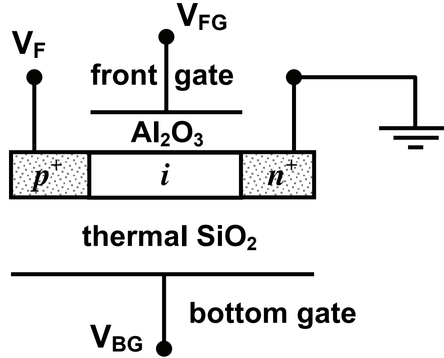


Figure 6.11: Schematic representation of the recombination-current measurement setup.

recombination components and therefore independently extract recombination characteristics of the crystallized-silicon volume as well as the front- (i.e., poly-Si / Al_2O_3) and bottom- (i.e., poly- Si / SiO_2) interfaces, according to the method described in [144, 145].

We assume that the energy level of the recombination centres (i.e. volume traps originating from the grain boundaries or contaminations and at the oxide interfaces due to the dangling bounds) are located at mid-gap. Furthermore, the volume recombination lifetimes for electrons and holes (τ_n and τ_p respectively) are assumed to be equal, as well as the surface recombination velocities (s_n for electrons and s_p for holes).

To provide in the intrinsic region a low-injection condition which ensures the domination of the recombination- over the diffusion current, a low forward bias (V_F) has to be applied to the p-i-n junction.

According to the Shockley-Read-Hall theory and under the above mentioned assumptions the maximum recombination rate is expected when the concentrations of electrons and holes become equal:

$$n = p = n_i \exp\left(\frac{qV_F}{2kT}\right) \tag{6.1}$$

where n_i is the intrinsic carrier concentration, q is the elementary charge, and kT is the thermal energy.

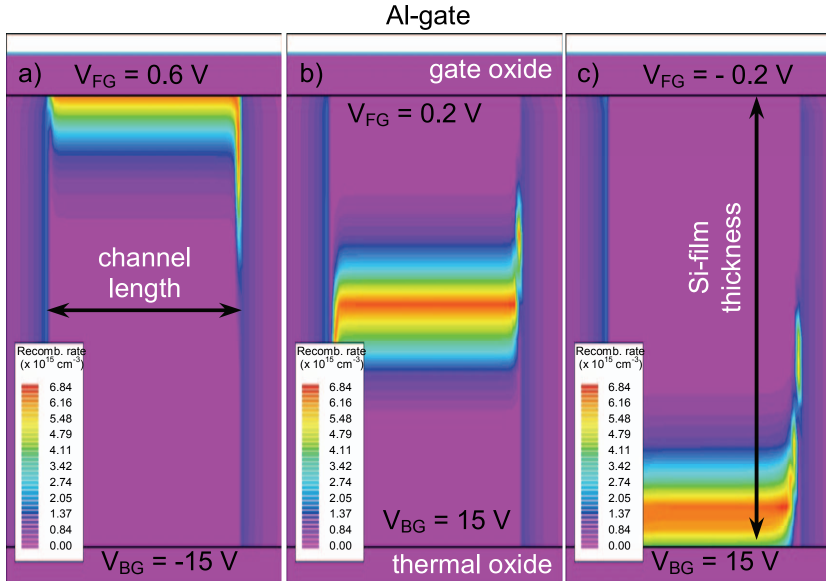


Figure 6.12: Modelled recombination in p-i-n diode at front- (a) and bottom- (c) interfaces; (b) - volume recombination.

To visualize the recombination processes the two-dimensional simulation of p-i-n structures has been done using SILVACO ATLAS code (shown in Figure 6.12). Clearly seen, when the p-i-n diode is slightly forward-biased ($V_F = 0.3$ V), the volume recombination current saturates if one of the interfaces is in strong accumulation and the other interface is in strong inversion. Such biasing condition prevents recombination at both interfaces and only results in volume recombination in the bulk (shown in Figure 6.12b), where the concentration of electrons and holes is equal according to (6.1). The recombination at the front- and at the bottom interface can only occur if the same condition (6.1) is met at one of the corresponding interfaces Figure 6.12a,c).

6.4.2 Fabrication of p-i-n diodes

The crystallized silicon films were initially patterned, to form islands. The boron and arsenic implantation and dopant activation was done in the same way as described in Section 6.3.1.

TFT process steps	technique	temperature
a-Si deposition	LPCVD	550 °C
lines patterning	wet etching	R.T.
a-Si deposition	LPCVD	550 °C
Si crystallization	laser crystallization	
Si-film patterning	wet etching	R.T.
S/D doping	ion implantation	R.T.
dopant activation	laser annealing	
Al_2O_3 gate deposition	ALD	300 °C
contact openings	wet etching	R.T.
metallization	Al sputtering	R.T.
Al patterning	wet etching	R.T.
post metall. anneal	in H_2O/N_2 for 10 min.	400 °C

Figure 6.13: Process steps used for the fabrication of p-i-n diodes and TFTs with alumina front gate.

A 16-nm thick Al_2O_3 gate dielectric layer was grown by ALD at a temperature of 300 °C. The wafer was subsequently exposed to $Al(CH_3)_3$ (Trimethylaluminum, or TMA) and H_2O, with an N_2-purge cycle in between [28]. The equivalent oxide thickness (EOT) of the alumina film was estimated at 7 nm. Finally, contact openings in the Al_2O_3 were etched in 0.1 % HF solution. The front- and backside were metallised by sputtering a 1-µm thick Al layer, patterned at the front side (defined by photolithography and wet etched) - providing metal contacts to the p- and n-type regions and forming the gate electrode. The post metallization anneal was done in H_2O/N_2 ambient for 10 minutes at 400 °C. The p-i-n diode fabrication process is summarized in Figure 6.13.

All electrical measurements were performed on a Karl Suss MicroTec PM300 Manual Probe Station equipped with a Keithley 4200 SCS.

6.4.3 Measured recombination on p-i-n diode

The recombination current dependence versus gate voltage can be used to extract carrier lifetime in the bulk and surface recombination rates at the interfaces [145].

Typical front- and bottom-gate measurements of the recombination current in p-i-n diode with the intrinsic region of 110 μm thick, 10 μm long and 50 μm wide at a forward-bias V_F = 0.3 V are shown in Figure 6.14. The front-gate voltage ranged from -0.2 V to 0.9 V, and the bottom-gate voltage from -30 V to 30 V. The high values of recombination currents if one interface is in a strong accumulation while the other interface is in a strong inversion (corresponding to the currents plateaus (I_{plateu}) on the left- and right-hand sides in Figure 6.14) confirm that volume recombination dominates in the crystallized films (schematically shown in Figure 6.12b). The volume recombination lifetimes could be calculated from:

$$\tau_v = \frac{q t_{eff} W L n_i}{I_{plateu}} \exp\left(\frac{qV_F}{2kT}\right) \tag{6.2}$$

where t_{eff} is the effective film thickness at the chosen measurement conditions ≈ 20 nm, and L and W are the length and width of intrinsic region, respectively,.

It is also possible to extract surface recombination rates from the current peaks (I_{front}, I_{back}), by proper biasing the front- and bottom-gates (as schematically shown in Figure 6.12a,b):

$$s_{f,b} = \frac{I_{front,back}}{qWLn_i \exp\left(\frac{qV_F}{2kT}\right)} \tag{6.3}$$

The extracted recombination characteristics of silicon films crystallized with different laser energies using the theory from [145] are shown in Table 6.2. A decrease of the volume- ($1/\tau_v$) and front-interface (s_f/t_{Si}, where t_{Si} is the Si film thickness) recombination (i.e., improvement of the layer quality) with increasing the laser energy is observed, whereas the bottom-interface recombination (s_b/t_{Si}) remains less affected. The latter can be

explained by a slight dependence of the bottom-interface quality on the laser treatment conditions for given laser powers. For lower powers, one can expect that a fraction of *a*-Si or fine-grained poly-Si remains at the bottom of the film (partial melting regime, shown in Figure 6.1a).

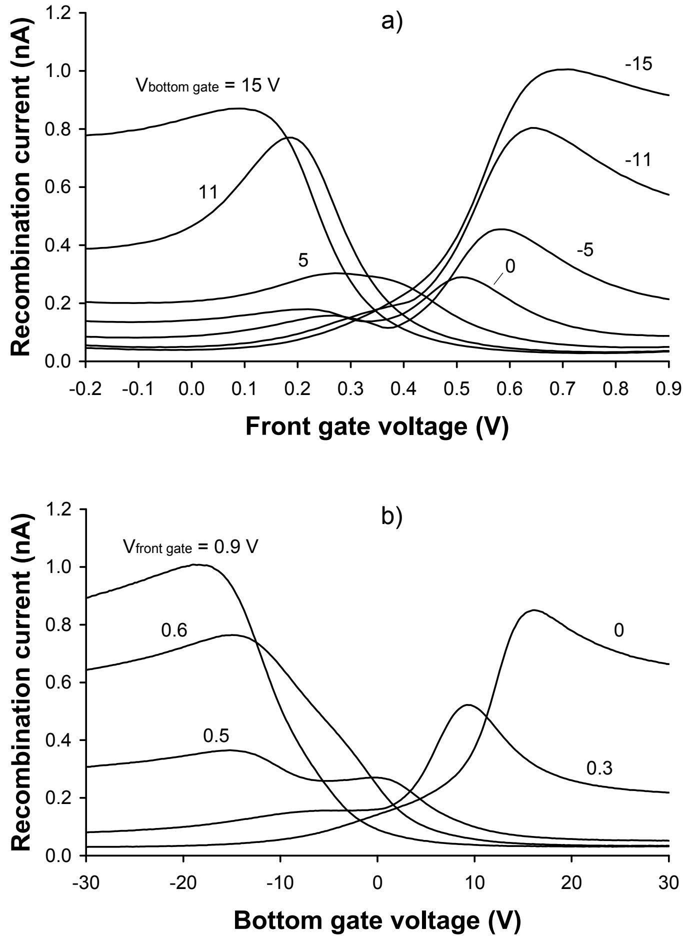


Figure 6.14: Recombination current of gated p-i-n diodes at $V_F = 0.3$ V (W = 50 µm; L = 10 µm; silicon film thickness 110 nm; crystallization laser energy 1.0 J/cm²) as a function of: (a) front-gate bias at various bottom-gate voltages; (b) bottom-gate bias at various front-gate voltages.

	This work			UNIBOND SOI	ZMR SOI
Laser energy during crystallization, (J/cm^2)	0.9	1.0	1.2	-	-
Volume recombination lifetime, τ_v (ns)	1.8	4.8	4.5	$\geq 10^5$	36
Front interface recombination velocity, s_f (cm/s)	174	143	121	6*	< 30*
Bottom interface recombination velocity, s_b (cm/s)	53	64	69	2	< 30

*The front SiO_2 gate oxide was thermally grown.

Table 6.2: Recombination parameters of crystallized silicon thin films.

p-i-n devices realized in this work are compared with p^+-p-n^+ and n^+-n-p^+ gated-diodes fabricated on UNIBOND and ZMR SOI substrates, respectively [145]. The recombination characteristics are in the same order as those of devices fabricated on a SOI film, made by the laser zone-melting re-crystallization (ZMR) technique. However, the higher level of the front-interface recombination (i.e., deteriorated interface quality) is likely due to the use of the low temperature ALD Al_2O_3 as the gate dielectric, in contrast to the thermally grown SiO_2 used for the Si-SiO_2 bottom interface.

One can conclude that in our devices the recombination current is determined by the volume component, similar to ZMR devices ($1/\tau_v > s_f/t_{Si} + s_b/t_{Si}$). In comparison, the high quality of silicon films in UNIBOND devices ensures a negligible contribution of the volume component, therefore the recombination current is determined mainly by surface recombination. The surface and volume recombination characteristics are improved by using higher laser crystallization energy.

6.5 TFTs with Al_2O_3 gate oxide

6.5.1 TFT fabrication

The TFTs with low-temperature 16-nm thick Al_2O_3 gate dielectric layer (EOT = 7 nm) grown by ALD, were fabricated in the same process flow as

p-i-n diodes described in Section 6.4.2. The same implantation doses of boron (1×10^{15} cm^{-2}) and arsenic (4×10^{15} cm^{-2}) ions at acceleration voltage of 55 keV were used to form P- and N-type regions for the source and drain. The dopant activation was done in the same way as described in Section 6.3.1. Similarly, sputtered 1-μm thick Al layers were used for front- and backside metallisation. The front side was patterned (using photolithography and wet etched) to provide the metal contacts to the source/drain regions and to form the gate electrode. Finally, the same post metallization anneal was done in H_2O/N_2 ambient for 10 minutes at 400 °C. The complete fabrication process is summarized in Figure 6.13.

Due to process failure, there is no complete sample series of NMOS TFTs, therefore, the data for parallel n-type transistors with alumina gate dielectrics are missing.

6.5.2 TFT characterization

The field effect mobility was calculated from transconductance g_m in the linear region at low source-drain voltage (V_{DS}) using the following equation [140]:

$$\mu_{FE} = \frac{L g_m}{W C_{ox} V_{DS}} \tag{6.4}$$

where C_{ox} is the gate oxide capacitance per unit area, L and W are the channel length and width, respectively, and

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS}=0.1V} \tag{6.5}$$

Here I_D is the drain current and V_{GS} is the gate voltage.

The measurements were done by varying the Al-front gate voltage with the Si-bottom gate (i.e. the substrate) grounded. The latter is the Si substrate separated from the TFT by the 0.9-μm thermal oxide. The device channels were undoped for both p- and n-channel TFTs. The measurements were done on devices with channels oriented *perpendicular* (p- and n-type) and *parallel* (p-type) to the laser scanning direction (or to the grain boundaries).

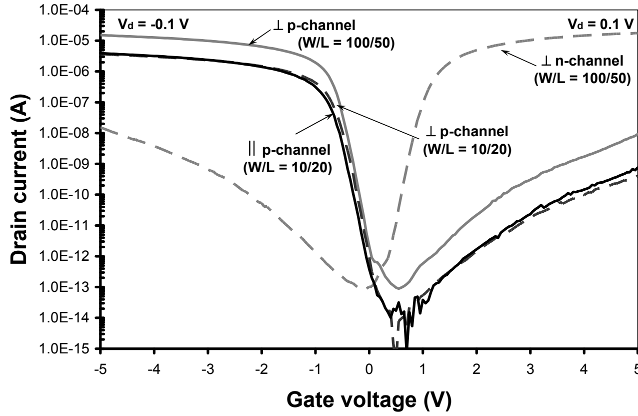


Figure 6.15: Transfer characteristics measured for P-channel and N- channel front-gate TFTs at a drain voltage of -0.1V or 0.1V.

Figure 6.15 shows typical transfer characteristics obtained at a drain voltage of -0.1 V for p-channel TFTs and 0.1 V for n-channel TFTs. The channel sizes (W/L) were 100 µm / 50 µm and 10 µm / 20 µm. Excellent I_{on}/I_{off} ratios over 10^8 are obtained as well as steep subthreshold slopes. The high off-state leakage currents are due to the gate-induced-drain-leakage

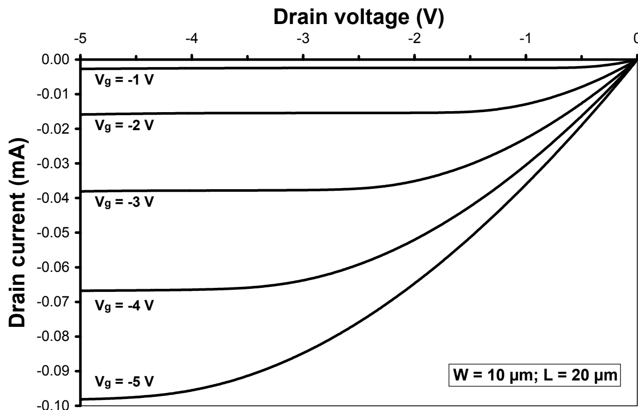


Figure 6.16: Output characteristics measured for P-channel TFT (W / L = 10 µm / 20 µm) at different gate voltages.

Symbol	N-type ⊥-TFT	P-type ⊥-TFT	P-type ||-TFT	P-type ||-TFT
TFT channel sizes (W/L)	100/60	100/60	10/20	10/20
Laser energy during crystallization, (J/cm^2)	1.0	1.0	1.0	1.2
Threshold voltage, V_T (V)	0.85	-0.58	-0.59	-0.7
On-to-off current ratio, I_{on}/I_{off}	> 10^6	> 10^6	> 10^6	> 10^6
Subthreshold slope, S (V/dec)	0.16	0.13	0.14	0.08
Front-side field effect mobility, $\mu_{FE, front}$ (cm^2/Vs)	62	46	52	62
Bottom-side field effect mobility, $\mu_{FE, bottom}$ (cm^2/Vs)	130	70	87	136

Table 6.3: Performance of TFTs with Al_2O_3 gate oxide.

(GIDL) caused by band-to-band tunnelling in the gate/drain overlap region [146-148]. This issue is typical for TFTs with ultra-thin gate oxide, and more pronounced when the interface state density is high; and in practice can be solved by applying a small drain off-set. The output TFT characteristics (Figure 6.16) exhibit typical linear-saturation curves for the drain current at various gate voltages. The summarized transistor characteristics are shown in Table 6.3.

At first glance the front-side mobility exhibits lower values than those reported in [101, 119, 120, 124, 149], where a thicker silicon oxide gate dielectrics were used. However, it is well known that the utilization of the high-*k* materials a gate dielectric reduces channel mobility. There are various physical scattering mechanisms considered to be responsible for mobility degradation. For instance, in [150] the authors claimed the surface phonon scattering to be the primary cause of electron mobility degradation. The proposed use of a mid-gap metal-gate shows an improvement of the mobility values due to the screening of the surface phonon-electron interaction [150].

It should be emphasized that in this work a thin (16 nm) Al_2O_3 gate dielectric deposited at low temperatures was applied. However, before the deposition of ALD Al_2O_3, the thin interfacial layer of native oxide was

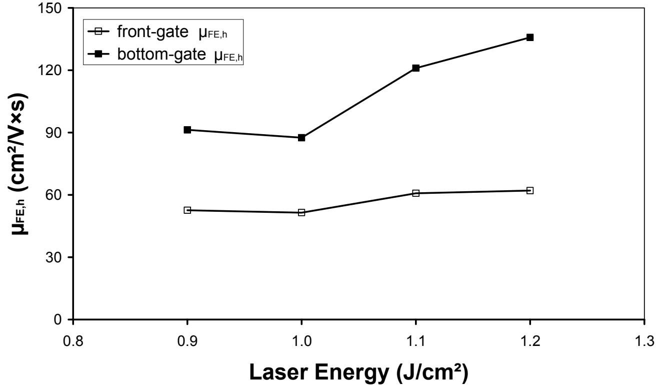


Figure 6.17: Field-effect front- and bottom-gate mobility for holes measured in p-channel TFTs (W / L = 10 µm / 20 µm) at different laser crystallization energies.

unavoidably formed. Therefore, the created multilayer gate stack has besides Al_2O_3/Al-gate interface an additional SiO_2/Al_2O_3 interface located very near to the channel due to the ultrathin interfacial SiO_2 layer. The reduced mobility in such layer stack was explained in [151] as due to the remote charge scattering of the charge carriers from fixed charges at the mentioned interfaces and in the volume of Al_2O_3 gate dielectric. To reduce the influence of fixed charges it is proposed to use a controllably grown 1-nm thick interfacial SiO_2 layer on the crystallized film [151].

Figure 6.17 represents the front- / bottom-gate field-effect mobility for holes at different laser crystallization energies. In this case, the TFT channels were oriented *parallel* to the laser scanning direction (or to the grain boundaries). One can clearly observe a significant difference between the front- and bottom-gate channel mobilities (shown also in Table 6.3) for both holes and electrons (similar to the recombination measurements results, shown in Section 6.4.3), indicating a better interface quality between the crystallized silicon and the bottom-gate dielectric. Additionally, carrier mobility is suppressed by the high surface roughness of the crystallized silicon film. A decreased value of the bottom-gate mobility, $\mu_{FE,h}$, at lower

energies probably indicates incomplete melting of the bottom part of the film due to the insufficient energy (see partial melting regime in Section 6.2.1).

To reach a higher value of the front-gate channel mobility, it is essential to reduce the influence of various scattering mechanisms and to improve the surface quality of the gate oxide by improving the ALD Al_2O_3 layer quality.

6.6 TFTs with SiO_2 gate oxide

It is reported a significant improvement in TFT performance when using silicon oxide as a gate dielectric instead of Al_2O_3 [151]. To evaluate the effect of silicon oxide utilization on the same laser crystallized silicon films, the devices with SiO_2 gate, deposited at low-temperatures, were investigated.

6.6.1 TFT fabrication

Similarly to the long diffusion area test structures (Section 6.3.1), thin film transistors were fabricated on patterned silicon films primarily crystallized with laser energy densities of 1.0 J/cm^2. The same implantation

TFT process steps	technique	temperature
a-Si deposition	LPCVD	550 °C
lines patterning	wet etching	R.T.
a-Si deposition	LPCVD	550 °C
Si crystallization	laser crystallization	
Si-film patterning	wet etching	R.T.
S/D doping	ion implantation	R.T.
dopant activation	laser annealing	
SiO_2 gate deposition	ICPECVD	150 °C
contact openings	wet etching	R.T.
metallization	Al sputtering	R.T.
Al patterning	wet etching	R.T.
post metall. anneal	in H_2O/N_2 for 10 min.	400 °C

Figure 6.18: Process steps used for the fabrication of TFTs with SiO_2 gate oxide.

conditions were used to form p- and n-type regions for the source and drain. Then the same dopant activation process was applied.

A 100-nm thick SiO_2 gate dielectric layer was deposited by means of remote inductively coupled plasma enhanced chemical vapour deposition (ICPECVD) in Ar-N_2O-SiH_4 plasma at 150 °C and pressure 1 Pa. The gas phase contained 0.08% of SiH_4 and 18% of N_2O - see [43] and [44] for more details. The thickness of the deposited oxides was determined by a Woollam M2000U spectroscopic ellipsometer (SE) and was confirmed by *C-V* measurements.

Then, contact openings in the SiO_2 were etched in a buffered hydrofluoric acid (BHF) solution. The front- and back-side were metalized by sputtering a 1-µm thick Al layer, patterned at the front side (defined by photolithography and wet etched) - providing metal contacts to the source/drain regions and forming the gate electrode. The post metallization anneal was done in H_2O/N_2 ambient for 10 minutes at 400 °C. The TFT fabrication process is summarized in Figure 6.18.

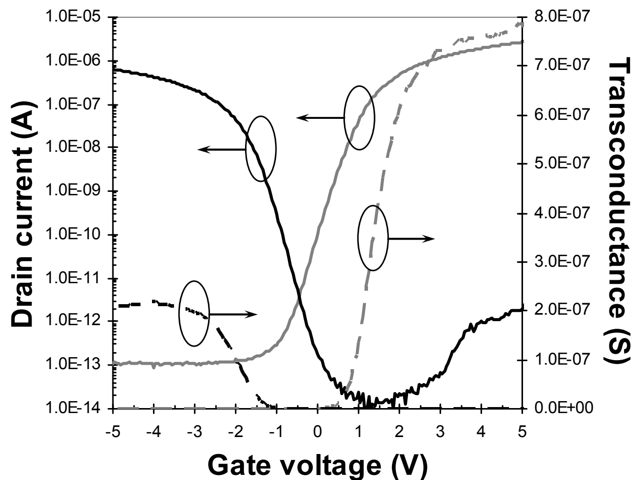


Figure 6.19: Transfer characteristics measured for parallel n-channel and p-channel TFTs (W / L = 10 µm / 20 µm) at a drain voltage of 0.1 V or -0.1 V. Laser crystallization energy was 1.0 J/cm².

Symbol	N-MOS		P-MOS	
	‖-TFT	⊥-TFT	‖-TFT	⊥-TFT
TFT channel sizes (W/L)	10/20	10/20	10/20	10/20
Threshold voltage, V_T (V)	1.5	3.6	-2.0	-4.1
On-current, I_{on} (μA)	35.1	6.1	7.6	1.5
Typical I_{on} full range variation (%)	8.2	9.3	7.5	8.5
Subthreshold slope, S (mV/dec)	308	359	275	383
Field effect mobility, μ_{FE} (cm^2/Vs)	405	145	128	89

Table 6.4: Performance of TFTs with SiO_2 gate oxide.

6.6.2 TFT characterization

The field effect mobility was calculated from transconductance g_m in the linear region at low source-drain voltage (V_{DS}) as described in Section 6.5.2. The measurements were done also by varying the Al-front gate voltage with

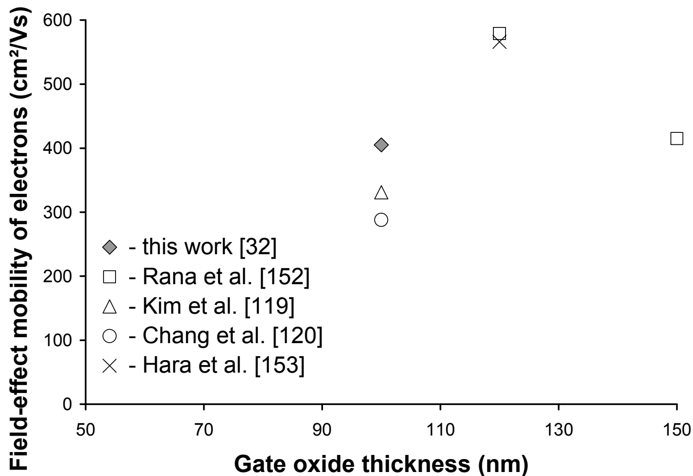


Figure 6.20: Comparison of the field-effect electron mobilities measured in TFTs with channels fabricated using different laser crystallization techniques.

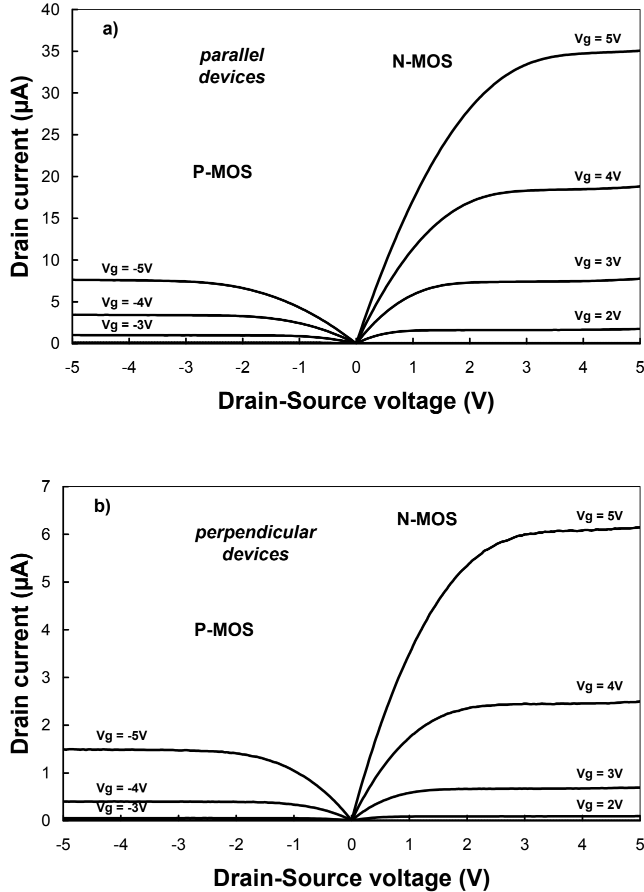


Figure 6.21: Output characteristics measured for a) parallel and b) perpendicular n-channel and p-channel TFTs (W / L = 10 µm / 20 µm) at different gate voltages. Laser crystallization energy was 1.0 J/cm^2.

the Si-bottom gate (i.e. the substrate) grounded. The device channels were undoped for both p- and n-channel TFTs.

Figure 6.19 shows typical transfer characteristics obtained at a drain voltage of -0.1 V for p-channel TFTs and 0.1 V for n-channel TFTs. For all the measured TFTs, the channels were realized in both *perpendicular* and *parallel* orientations to the laser scanning direction (or to the random grain boundaries), and the channel sizes (*W*/*L*) were 10 µm / 20 µm.

A correct orientation of transistors with respect to the grain boundaries is essential. The *parallel* TFTs show superior mobility for both N- and P-MOS transistors, as listed in Table 6.4. The TFTs with channels oriented *parallel* to the random grain boundaries additionally exhibit a lower subthreshold slope (Table 6.4) and little location dependence. Furthermore, the mobility of the present TFTs using ICPECVD SiO_2 is significantly higher than earlier fabricated TFTs with ALD Al_2O_3 (see Section 6.5). We attribute this mobility enhancement to the use of a thick high-quality SiO_2 gate dielectric [44] in contrast to the earlier used thin Al_2O_3 [31]. Al_2O_3 has also shown to yield lower mobilities in the case of TFTs on monocrystalline Si [151]. We compare the found N-MOS mobility values to literature values in Figure 6.20. Here, the mobilities are plotted against dielectric thickness, as it is commonly observed that the field effect mobility tends to decrease for thinner dielectrics. The mobility found in our work is in fact very competitive to literature values when regarded in this perspective; higher mobilities are only reported using thicker dielectrics [119, 120, 152, 153].

The output characteristics (Figure 6.21) exhibit typical linear-saturation curves for the drain current at various gate voltages. Thus, as it follows from the transfer and output characteristics, the orthogonal devices show a lower mobility, strongly dependent on the placement of the device with respect to the grain boundaries: an improper placement leads to lower on-currents.

As schematically shown in Figure 6.3, laser crystallization with underlying preformed *a*-Si lines enables the formation of grains, enlarged in laser scanning direction, with grain boundaries dominantly located in between the line positions. A series of twenty TFTs with predetermined channel locations (oriented *perpendicular* to the laser scanning direction and to the grain boundaries) was manufactured. The channel sizes (W/L) were 12 µm / 2 µm. The channel of each next transistor was shifted in the x-direction for 0.2 µm with respect to the position of the previous transistor in the same series. This gradual channel shift ensures the existence of TFTs with random grain boundaries located in the channel, and devices with much less boundaries or even grain boundary free channels.

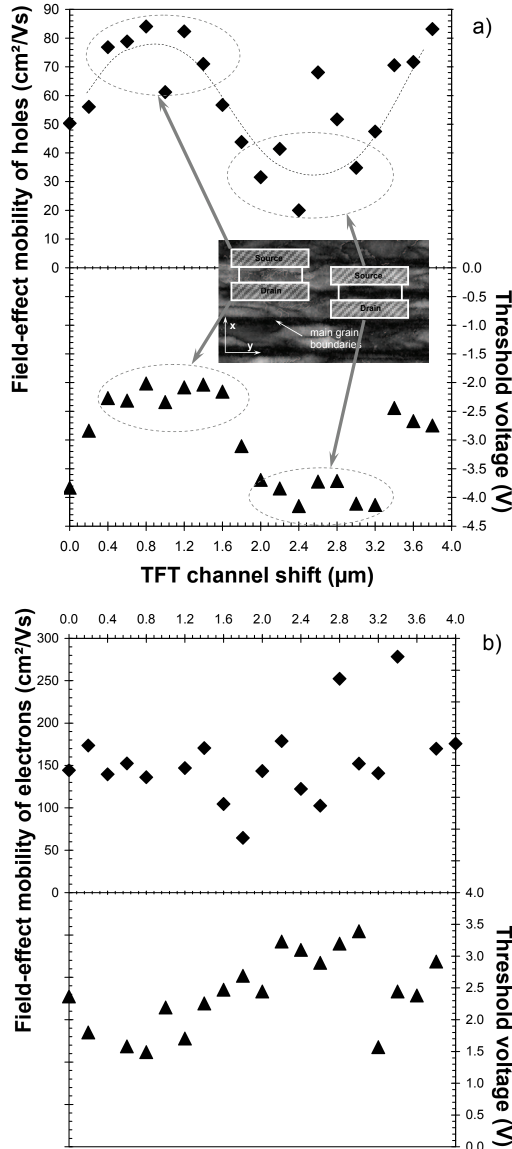


Figure 6.22: Location-dependent field-effect mobility of holes ($\mu_{FE,h}$) a) and electrons ($\mu_{FE,e}$) b) and threshold voltage measured for perpendicular p-channel and n-channel TFTs ($W / L = 12\ \mu m / 2\ \mu m$, laser crystallization energy 1.0 J/cm^2). Between neighbouring devices the TFT channel is shifted with a step $\Delta x = 0.2\ \mu m$ in the x-axis direction, see Figure 6.3. Dashed lines are drawn to guide the eye.

The measured mobility and threshold voltage values (Figure 6.22) show a performance enhancement of the TFTs having channels placed in between the random grain boundaries. This behaviour is clear pronounced in case of the p-channel TFT (Figure 6.22a) while in n-channel TFTs it is diminished for this sample series (Figure 6.22b), probably due to the larger number of formed random grain boundaries per N-type device area.

6.7 CMOS inverters and ring oscillators

To perform a dynamic characterization of the TFTs, we designed and fabricated CMOS inverters and 51-stage ring oscillators, as shown in Figure 6.23. For a basic CMOS inverter, the channel widths for p- and n-channel TFTs were 3 μm and 2 μm, respectively, and the channel lengths were 2 μm for both transistor types. To avoid loading down the ring oscillator, an output buffer stage was designed. It consisted of one basic inverter and an additional inverter stage having P- and NMOS transistors with W/L = 50 μm / 2 μm.

Figure 6.24a shows the basic inverter transfer characteristics for a supply voltage (V_{DD}) of 5 V. The inverter exhibits an abrupt full-range

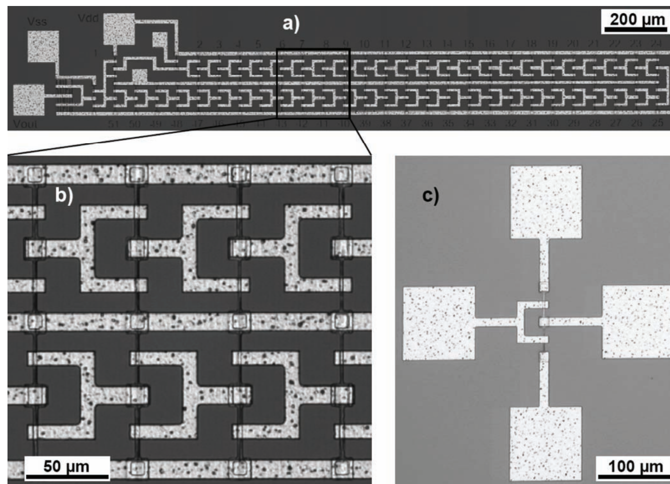


Figure 6.23: The optical image of a) 51-stage ring oscillator (eight stages are zoomed-in in (b)), and c) CMOS TFT inverter.

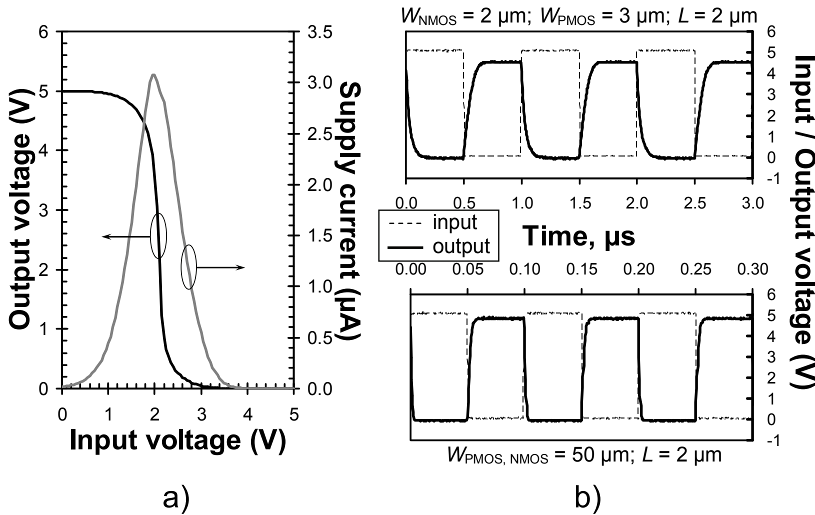


Figure 6.24: Transfer characteristics of CMOS TFT inverters (a) static and (b) dynamic at V_{DD} = 5 V (the TFT-channels are oriented parallel to the grain boundaries).

output voltage switch at an input voltage around 2.1 V. The dynamic output characteristics of the basic inverter and the inverter with wider channels ($W_{NMOS,\ PMOS}$ /L = 50 µm / 2 µm) are compared in Figure 6.24b. The extracted rise and fall times are 103 µs and 80 µs for the basic inverter, and 3.9 µs and 1.9 µs for the inverter with wider channels. These values are however conservative estimates of the real switching speed, given the large parasitic capacitance present in this measurement.

The ring oscillators exhibit stable oscillations with frequencies in the MHz-range with the TFT-channels oriented *parallel* to the grain boundaries. None of the ring oscillators with *perpendicularly*-oriented TFTs oscillates at all. This is most probably due to the large threshold voltage deviation for each TFT (see Figure 6.22) caused by the grain boundaries perpendicular to the current flow. Figure 6.25 shows the output of an unloaded 51-stage CMOS ring oscillator. In addition to the fundamental oscillation frequency of 0.68 MHz, odd higher harmonics (1.97 MHz and 3.27 MHz) were measured for the same ring oscillator, in line with reports in [154, 155]. The

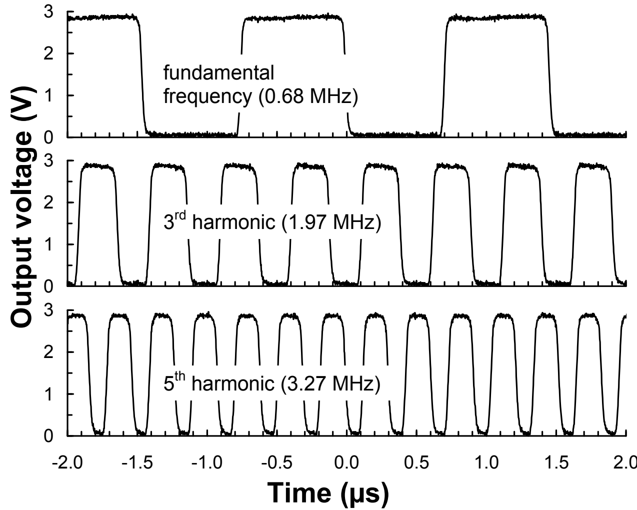


Figure 6.25: Three oscillation waveforms, measured for the 51-stage CMOS ring oscillator at a supply voltage $V_{DD} = 5$ V ($W_{NMOS} = 2$ µm; $W_{PMOS} = 3$ µm; $L = 2$ µm; the TFT-channels are oriented parallel to the grain boundaries).

V_{DD} dependence of the oscillation periods for the three harmonics is shown in Figure 6.26. Using the fundamental frequency, the propagation gate delay t_{pd} amounts to 14.4 ns, obtained by the following equation [156]:

$$t_{pd} = \frac{nT}{2N} \tag{6.6}$$

where T is the period of the oscillation, N is the number of stages and n is the number of harmonic.

Similarly to the experiment with shifted TFTs (see Figure 6.22), a series of eleven ring oscillators with predetermined channel locations (oriented *parallel* to the laser scanning direction and to the grain boundaries) was fabricated. Channels of all transistors in every next ring oscillator were shifted perpendicularly to the random grain boundaries for 0.4 µm with respect to the channel positions in the previous ring oscillator of the series. As stated earlier, this shift ensures the existence of oscillators with and without random grain boundaries in the channels.

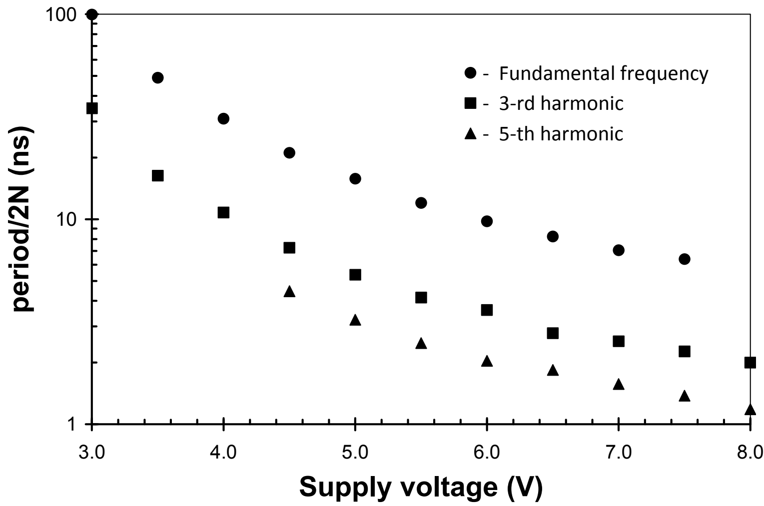


Figure 6.26: Dependence of the oscillation period on V_{DD} for different harmonics.

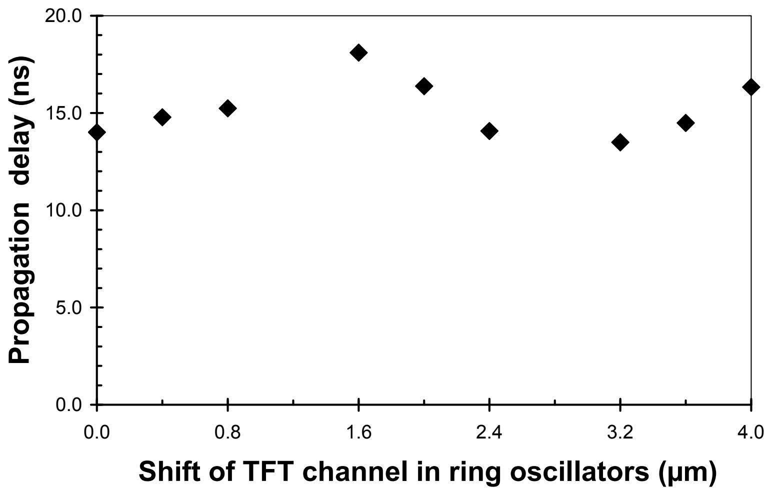


Figure 6.27: Location-dependent propagation gate delay determined with the fundamental frequency mode for the ring oscillators with parallel TFT channels (WNMOS = 2 µm; WPMOS = 3 µm; L = 2 µm).

Although the current flow in all these ring oscillators is parallel to the boundaries, we still observe a deviation in the device performance, leading to a lower propagation gate delay when fewer boundaries are expected to be present in the channels (Figure 6.27). This demonstrates the effectiveness of the device positioning method proposed in this work.

6.8 Conclusion

Amorphous silicon films with underlying *a*-Si lines were deposited on thermally grown SiO_2. The green-laser crystallization showed that the pre-forming leads to large-grain poly-Si films with the grain boundaries mostly oriented along the underlying *a*-Si lines.

After dopant activation with a similar green laser system, the sheet resistance is lower and shows a lower variability for devices oriented *parallel* to the random grain boundaries than for *perpendicularly*-oriented devices. Additionally, heavily As- and B-doped silicon films exhibit high doping activation levels.

The recombination currents, measured in forward biased gated p-i-n diodes, show a domination of the volume recombination in the crystallized silicon film. The use of higher laser fluence leads to improved recombination characteristics in the crystallized silicon films.

High-performance p- and n-channel poly-Si TFTs were fabricated using pre-formed *a*-Si, green-laser crystallization and activation, and a low-temperature gate dielectric (ALD – Al_2O_3 and ICPECVD – SiO_2). The TFTs oriented *parallel* to the underlying *a*-Si lines (and therefore to the grain boundaries) exhibit significantly better electrical performance than the *perpendicularly*-oriented devices. Additionally, the devices with alumina as a gate dielectric are inferior to the devices with silicon oxide gate in terms of mobility.

51-stage CMOS ring oscillators with *parallel* TFTs were fully operational and showed a slight improved performance if all TFT-channels were positioned in between the random grain boundaries. In contrast, the

ring oscillators made of the *perpendicularly*-oriented TFTs were not functioning.

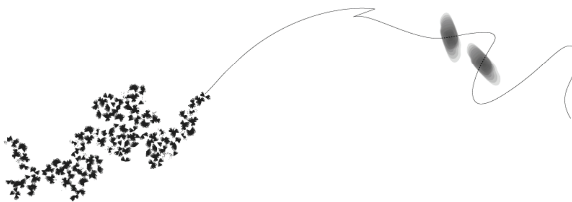
The described low-temperature fabrication method can be further developed for low-temperature CMOS post-processing, after replacing the LPCVD step at 550 °C by e.g. plasma-enhanced CVD of *a*-Si at temperatures lower than 400 °C. This CMOS process can be employed for large-area TFTs as well as in 3-D electronics due to its low thermal budget.

“Cogitationis poenam nemo patitur”

“Nobody should be punished for his thoughts”

Roman Law (D. 48. 19. 18)

7 Conclusions and recommendations



7.1 Conclusions

The goal of this work was to investigate the critical low-temperature processing steps required for monolithic 3-D integration of ICs (e.g. deposition of semiconductor and dielectric films, and performance enhancement of silicon films).

A custom-designed cluster system was applied to fabricate the functional multilayer stacks with Si-ND's embedded in dielectric layers. The used deposition techniques (i.e. ALD, LPCVD, ICPECVD) and the expected mechanisms of silicon nucleation and growth are discussed. An increase in the growth rate and in the density of silicon nanodots deposited with Si_3H_8 (Silcore®) as a precursor gas in comparison to Si_2H_6 is demonstrated.

The structures used for memory application were fabricated at temperatures below 425 °C except for the thermally grown silicon oxide layer. Good program and erase behaviour together with appreciable retention and endurance were measured on realized floating-gate memory devices.

Optically active multilayer stacks consisting of silicon nanodots embedded in alumina were processed at temperatures below 325 °C. The Si-NDs exhibit quantum confined near-infrared photoluminescence and electroluminescence. The PL emission spectra show a "blue-shift" with decreasing the nanodot layer thickness. The photoluminescence quantum efficiency for realized multilayer stacks is estimated to be 0.3%.

To improve the electronic device characteristics and to ensure the low thermal budget during processing (i.e. during 3-D integration) the green-laser treatment was used for crystallization of silicon films and dopant activation.

Laser crystallization of pre-formed initial *a*-Si films leads to large-grain poly-Si films with the predicted location of the random grain boundaries mostly oriented along the laser scanning direction. Consequently, the sheet resistance is lower and shows a lower variability for devices oriented *parallel* to the random grain boundaries than for *perpendicularly*-oriented

devices. Additionally, heavily As- and B-doped silicon films exhibit high doping activation levels.

The recombination currents, measured in forward biased gated p-i-n diodes, show a domination of the volume recombination in the crystallized silicon film. The use of higher laser fluence leads to improved recombination characteristics in the crystallized silicon films.

High-performance p- and n-channel poly-Si TFTs were fabricated using pre-formed *a*-Si, green-laser crystallization and activation, and a low-temperature gate dielectric (ALD – Al_2O_3 and ICPECVD – SiO_2). The TFTs oriented *parallel* to the underlying *a*-Si lines (and therefore to the grain boundaries) exhibit significantly better electrical performance than the *perpendicularly*-oriented devices. Additionally, the devices with alumina as a gate dielectric are inferior to the devices with silicon oxide gate in terms of mobility.

51-stage CMOS ring oscillators with *parallel* TFTs were fully operational and showed a slightly improved performance if all TFT-channels were positioned in between the random grain boundaries. In contrast, the ring oscillators made of the *perpendicularly*-oriented TFTs were not functioning.

7.2 Recommendations

1. To gain further insight about the initial phase of silicon nucleation on various substrate materials the “in-situ” spectroscopic ellipsometric measurements has to be done. Therefore, the spectroscopic ellipsometer has to be installed in reactor 2 (that was not yet available in experiments described in this work).

2. As mentioned in section 5.4.1 it was not possible to observe the complete “blue-shift” of the luminescence maximum with the decreasing nanodot layer thickness. The oxide matrix (in this case Al_2O_3) leads to formation of Si=O bonds, with recombination in the oxygen related surface states dominating in small nanodots. A surface nitridation carried out just before and directly after Si-ND deposition could suppress the formation of

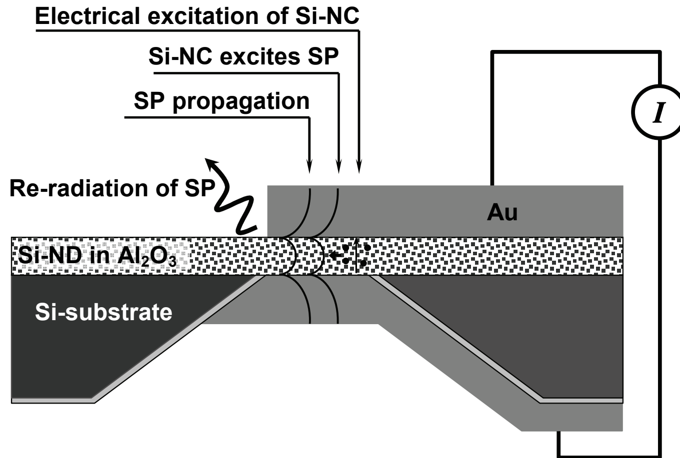


Figure 7.1: Schematic cross-section of metal-insulator-metal (MIM) surface plasmon polariton source. The MIM membrane consists of an alumina matrix with embedded silicon nanodots lying between two metal (gold) layers. Surface plasmons are launched by applying a bias across a membrane and propagate at the interfaces between a metal and dielectric.

interfacial oxide layer. It could be realized using a short NH_3-plasma treatment. This process is available in reactor 1.

3. The measured electroluminescence in multilayer stacks with embedded silicon nanodots and their CMOS back-end compatible low-temperature processing, makes these structures very attractive for generation of a surface plasmon polariton (shown in Figure 7.1). Our first research results on this issue are reported in [34, 87, 157, 158]. For the successful utilization of MIM structures as a light source it is required to translate the complete process flow to a CMOS back-end compatible one.

4. The low-temperature fabrication method described in chapter 6 can be further developed for low-temperature CMOS post-processing, after replacing the LPCVD step at 550 °C by e.g. plasma-enhanced CVD of *a*-Si at temperatures lower than 400 °C. This CMOS process can be employed for large-area TFTs as well as in 3-D electronics due to its low thermal budget.

Using green-laser crystallized silicon in combination with the low temperature deposition of the multilayer stacks, a variety of devices has to be fabricated on top of the conventionally made ICs. The influence of 3-D post-processing on the performance of the underlying circuits has to be investigated.

5. Although the grain boundaries are extremely undesirable in electronic devices, some of their properties could still be very useful. A significant light sensitivity was observed on the TFTs (e.g. output currents) having the grain boundaries located in the channel and oriented *perpendicularly* to the current flow direction. While the location of the regions with the maximum grain boundary concentration is known, the effect could be used to realise light sensors. The CMOS back-end compatibility, low temperature laser treatment and any new processing step, enables an easy 3-D integration of such devices for optical data transfer within ICs.

“Ex ipso fonte bibere”

"To drink from the same source"

Marcus Tullius Cicero

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“Ab ovo usque ad mala”

“From the egg right to the apples”

Quintus Horacius Flaccus

Summary

The number of transistors in integrated circuits is exponentially increasing over time, as predicted by Gordon Moore in the 1960s (e.g. 781 million transistors in the current Intel Xeon processor). This leads to higher computing power at a reduced cost per function. However, the future scaling perspective encounters several limiting factors, such as: an increased interconnect resistance-capacitance (RC) delay, enormous power densities – the so-called “power wall”, and exploding costs due to the high process complexity. Therefore, further functionality growth within conventional planar ICs would not be possible without compromising on performance or cost, requiring drastic changes in the production process. Three-dimensional (3-D) integration of ICs, as already foreseen in the same ’60s but thus far kept in the periphery of semiconductor technology, is nowadays gaining attention as an alternative to further lateral downscaling. It is highly attractive for application in mobile computing devices, where various functionalities have to be added to a single die to keep the system’s dimensions small.

The goal of this work was to develop techniques for the monolithic 3-D integration of ICs, in particular, by vertical integration of several active layers through sequential processing. Two main restrictions in this work were to keep the thermal budget of the processes low and to ensure the CMOS back-end compatibility. The research was focused on two key-processes: a) low-temperature deposition of semiconducting and dielectric films; and b) performance enhancement of silicon films by means of green laser crystallization and dopant activation in such films.

Studies of low-temperature deposition techniques (i.e. ALD, LPCVD, ICPECVD) were performed in a custom-designed cluster system, and were mainly focused on the formation of silicon nanodots as a functional layer for memory- and photonic applications. To obtain a high density of nanodots, Si_3H_8 (Silcore®) was used as a precursor gas. The custom-designed cluster system provides the possibility of depositing various layers in sequence without vacuum break, herewith allowing low-temperature formation of the multilayer stacks with embedded Si-nanodots.

The obtained non-volatile memory devices with Si-nanodot floating gates exhibit both good program and erase behaviour, with appreciable retention and endurance. Silicon nanodots exhibit quantum confined near-infrared photoluminescence and electroluminescence in optically active structures. The “blue-shift” of photoluminescence emission spectra was found to be more pronounced for smaller Si-nanodots.

Green laser irradiation was used for silicon film crystallization and dopant activation. During each laser pulse only a tiny fraction of the film was melted and then re-crystallized without heating of the complete wafer. It was found, that the additional use of pre-formed underlying *a*-Si films leads to large-grain poly-Si films with a predictable location of the random grain boundaries mostly oriented along the laser scanning direction. An important advantage of this method, compared to existing methods of grain boundary control, is the utilization of already existing process steps only, making this concept cheap and simple in terms of industrial application.

Sheet resistance measurements confirmed an anisotropic nature of a crystallized film with enhanced characteristics, measured on test devices oriented parallel to the laser scanning direction. High doping activation levels in heavily As- and B-doped silicon films were achieved. The volume recombination, estimated from the current measurements in forward biased gated p-i-n diodes, was found to be dominant in the crystallized silicon film.

High-performance p- and n-channel poly-Si TFTs were fabricated using laser crystallized silicon films and low-temperature deposition steps. Since the random grain boundaries are found at predictable positions, this allows

the transistor definition away from these boundaries. TFTs, manufactured in accordance to the described process, exhibit high field-effect carrier mobilities of 405 cm^2/Vs (NMOS) and 128 cm^2/Vs (PMOS). Thus, the proposed grain boundary control offers a combination of high mobility and low variability.

CMOS inverters and fully functional 51-stage ring oscillators were fabricated using the same process as TFTs. Ring oscillators with suppositional optimal location of TFT-channels showed improved performance; moreover those ring oscillators that were made of the perpendicularly-oriented TFTs were not functioning.

To conclude, the described processes can be employed for large-area TFT electronics as well as a functional stack layer in 3-D integration due to their low thermal budgets and their CMOS backend-compatibility.

"Intelligenti pauca"

"Voor iemand die begrijpt volstaan weinig woorden"

Samenvatting

Sinds de introductie van transistoren in geïntegreerde schakelingen (IC's) aan het begin van de jaren 60 van de vorige eeuw heeft het gebruik ervan een exponentiële groei doorgemaakt, precies zoals Gordon Moore voorspelde. Deze groei werd mogelijk gemaakt door steeds verder doorgevoerde miniaturisatie van de schakelingen. Hierdoor nam de rekenkracht van IC's toe (ter illustratie, de huidige Intel Xeon processors bevatten 781 miljoen transistoren). De mogelijkheid tot verdere verkleining wordt echter beperkt door verscheidene factoren, waaronder toenemende signaalvertraging in de bedrading door verhoging van de RC-tijd, het ontstaan van een enorme vermogensdichtheid – de zogenoemde "power wall" – en explosief toenemende productiekosten door de uiterst complexe aard van het proces. Daardoor is verdere functionaliteitstoename bij conventionele, platte IC's onmogelijk zonder doorvoering van veranderingen in het productieproces of compromissen in prestaties of kosten. Over driedimensionaal integreren bij IC's sprak men al in de jaren 60 van de vorige eeuw, maar dit werd door de halfgeleidertechnologie nog afgehouden. Tegenwoordig is er toenemende belangstelling voor. Het is een erg aantrekkelijke aanpak voor gebruik in mobiele computerapparatuur, waarbij uiteenlopende functies moeten worden toegevoegd aan een enkele chip waarvan de afmetingen klein moeten blijven.

Doel van het onderzoek was de ontwikkeling van monolithische 3D-integratie bij IC's, met andere woorden: verticale stapeling van verscheidene actieve lagen. De twee belangrijkste beperkingen hierbij waren het laag houden van de warmteontwikkeling en het garanderen van

compatibiliteit met het CMOS-productieproces. Het onderzoek richtte zich op de twee belangrijkste processen: A. Depositie op lage temperatuur van halfgeleider- en diëlektrische films. B. De verbetering van de prestaties van de silicium films door groene laserkristallisatie en doteringsactivering.

De onderzoeken naar depositieprocedés op lage temperatuur (ALD, LPCVD, ICPECVD) werden uitgevoerd in een speciaal daarvoor ontworpen clustersysteem. De procedés richtten zich voornamelijk op het vormen van silicium nanodots als functionele laag voor geheugentoepassingen en fotonische toepassingen. Om een hoge dichtheid aan nanodots te verkrijgen, werd Si_3H_8 (Silcore®) gebruikt als precursorgas. Met het clustersysteem werd opeenvolgende depositie van verschillende lagen mogelijk zonder het vacuüm te verbreken, waardoor op lage temperatuur meerdere lagen konden worden gestapeld met ingesloten Si nanodots.

De niet-vluchtige geheugencomponenten verkregen met een uit Si-nanodots bestaande zwevende poort, vertonen zowel goed invoergedrag als wisgedrag, met aanzienlijke retentie en duurzaamheid. Silicium nanodots vertonen door quantum beperkte, nagenoeg infrarode fotoluminescentie en elektroluminescentie in optisch actieve structuren. De "blauwverschuiving" van fotoluminescentie-emissiespectra bleek meer uitgesproken bij kleinere Si-nanodots.

Silicium films werden door middel van groene laserinstraling geactiveerd en gekristalliseerd. Elke laserpuls smolt slechts een minuscuul deel van de film. Daarna kristalliseerde die weer zodat niet het gehele substraat verhit hoefde te worden. Het bleek dat aanvullend gebruik van voorverwerkte amorfe Si-films leidt tot grofkorrelige poly-Si-films waarbij de positie van de belangrijkste korrelgrens goed te voorspellen is, als zijnde vooral langs de richting van de laserscan. Het belangrijkste voordeel van dit procedé ten opzichte van andere processen die de locatie van korrelgrenzen controleren, is dat het gebruikmaakt van bestaande procesonderdelen en geen nieuwe behoeft, waardoor het goedkoop en eenvoudig industrieel te gebruiken is.

Metingen aan de laagweerstand, gedaan met teststructuren parallel aan de laserscanrichting, bevestigden de anisotropische aard en verbeterde eigenschappen van de gekristalliseerde film. Hoge doteringsactiveringsniveaus werden bereikt met silicium films die waren gedoteerd met As en B. De recombinatie in het volume van de korrel, geschat aan de hand van stroommetingen aan in doorlaatrichting geschakelde, gated p.i.n.-dioden, bleek overheersend te zijn in de gekristalliseerde silicium film.

Er zijn hoogwaardige p- en n-kanaals poly-Si dunnefilmtransistoren (TFT's) gefabriceerd met behulp van lasergekristalliseerde silicium films en depositieprocedés bij lage temperaturen. Aangezien de belangrijkste korrelgrenzen op voorspelde posities bleken te liggen, konden transistoren zonder korrelgrenzen worden gedefinieerd. TFT's die zijn vervaardigd conform het hierboven beschreven proces vertonen een hoge veldeffectmobiliteit van 405 cm^2/Vs (NMOS) en 128 cm^2/Vs (PMOS). De korrelgrenssturing biedt een combinatie van hoge mobiliteit en lage variabiliteit.

Met hetzelfde procedé dat werd gebruikt voor TFT's werden tevens CMOS-inverters en volledig bruikbare 51-traps ringoscillatoren gefabriceerd. Ringoscillatoren met een optimale locatie van de TFT-kanalen vertoonden verbeterde prestaties. Bovendien waren de ringoscillatoren gemaakt van loodrecht op de laserscanrichting georiënteerde TFT's niet bruikbaar.

Concluderend kan worden gesteld dat de beschreven processen toegepast kunnen worden bij een groot deel van de TFT-elektronica en tevens voor functioneel gestapelde 3D-integratie, dankzij de lage substraattemperatuur tijdens fabricage en de goede compatibiliteit met het CMOS-productieproces.

“Feci quod potui, faciant meliora potentes”

"I have done what I could,
those who can - will do better"

List of publications

I. Brunets, J. Holleman, A. Y. Kovalgin, A. Boogaard, and J. Schmitz, "Low-Temperature Fabricated TFTs on Polysilicon Stripes," *IEEE Transactions on Electron Devices*, vol. 56, pp. 1637-1644, 2009.

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R. J. Walters, R. van Loon, I. Brunets, J. Schmitz, and A. Polman, "A Silicon-Based Electrical Source for Surface Plasmon Polaritons," presented at G4 Photonics, 2009.

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Factum est.